High Voltage AC Hot Carrier Test System

Application area: smart power supply systems

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For high power devices, a testbench that uses a DC stress condition is not an option (or can be a problem) due to e.g. heating problems of the device. To measure the degradation behavior, pulsed stress conditions can be used.

The AC Hot Carrier Test System has been constructed to deal with some of the above mentioned problems. It's a special set-up dedicated to measure the hot carrier degradation of integrated power transistors under switching conditions. This means that the gate of the device can be switched on-off with a certain frequency, pulse shape... while keeping the voltage at the drain fixed.

This system is an extension of the DC Hot Carrier System to the more realistic case of AC stress under various loading conditions. It 's possible to study the impact of AC stress parameters as pulse frequency, pulse width, rise and fall time,... on the degradation behaviour. Real life AC hot carrier stress can be performed on high power switches switching inductive, resistive and/or capacitive loads as they are present in a real circuit. The effect of cumulative stress can be investigated. The AC hot carrier measurements can be performed at low as well as high temperatures.

System description and specifications

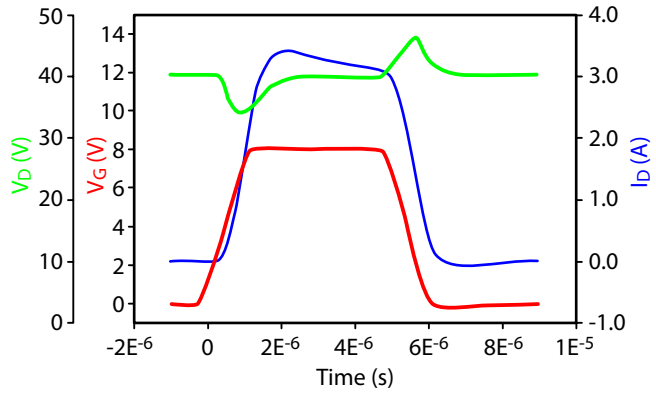
The test setup is only able to stress and characterise 1 transistor at a time due to the high power involved.

Parameter	Specification
Temperature range	-50°C ... 170°C
Temperature stability	0.5°C
Drain supply voltage	-120V ... 120V
Maximum drain supply current	25A
Gate pulse frequency range	< 20MHz
Gate pulse width range	10ns ... 999s
Gater pulse transition time	5ns ... 200ms
Gate pulse amplitude	-20V ... 20V
Maximum gate supply current	400mA
Measurement resolution	< 0.1%
Measurement capacity	1 sample

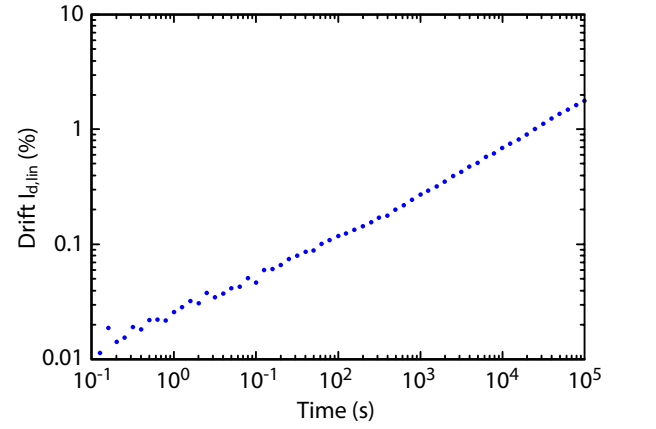
Measurement example

As an example the hot carrier degradation of a DMOS high voltage transistor is shown.

The top graph shows the V_D, V_G and I_D-signals as applied during the AC hot carrier experiment. The transistor was subjected to a constant drain voltage of 40V, while the gate voltage is pulsed. The gate pulse amplitude was 8V, with a pulse width of 5µs and a frequency of 250Hz (25% duty cycle). The fall and rise time of the pulses was 1µs. No load was applied during this degradation experiment. On the bottom graph, the drift of the linear drain current is shown as a function of time at a temperature of 20°C. The results out of this experiment were cross-checked with a DC Hot carrier measurement on the same type of sample.



V_D, V_G and I_D signals during AC hot carrier experiment



Drift of lineair drain current measured at 20°C

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