

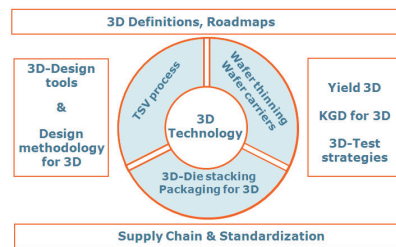


# 3D SYSTEM INTEGRATION

3D integration complements semiconductor scaling; it enables a higher integration density as well as heterogeneous technology integration. Using 3D chip stacking, it is possible to extend the number of functions per 3D chip well beyond the near-term capabilities of traditional scaling. The 3D strata may be realized using advanced CMOS technology nodes but may also exploit a wide variety of device technologies to optimize system performance. The goal of imec's 3D program is to concurrently explore the technology and design issues associated with several 3D application domains.

## SCOPE

The introduction of 3D technology in the microelectronic industry calls for innovations throughout the supply chain.



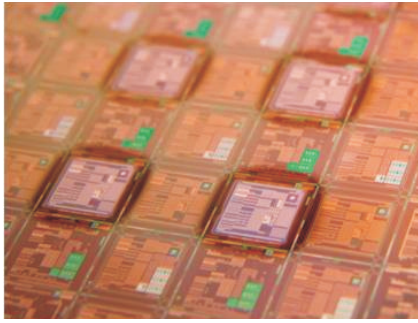
The technology needed for 3D stacking consists of three main processes: The through-Si via process, processes for bonding and thinning wafers on carriers, allowing for backside processing on thinned wafers and the actual chip stacking and stack packaging operations. Imec studies new technologies and materials for each of these areas.

Next to the technology, the design of 3D systems is a key topic of the 3D research program. 3D system design exploration steers the direction of the process development, and technology is an enabler for improved system design. A path finding flow is developed to study the system-level trade-offs at an early phase of the system design.

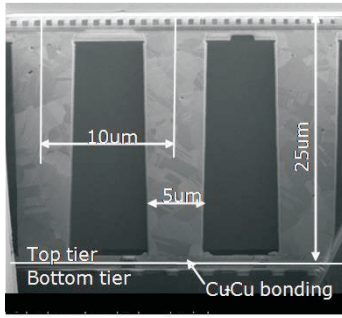
The 3D integration approach should be cost-effective and consider the potential compound yield risks by adopting the appropriate testing and known-good-die strategies. We also participate in road mapping and standardization activities where appropriate.

## THE PROGRAM PARTNERS

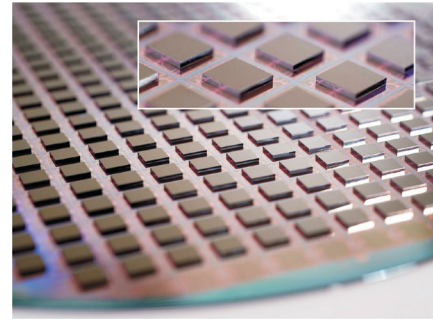
The partners in the program are IDM's, IC foundries, memory suppliers, "fablight" and "fabless" companies, OSAT's, EDA companies, process, test and metrology equipment suppliers and material suppliers, reflecting the complexity of the 3D microelectronic supply chain. A good alignment between these actors is required to make 3D system integration an industrial reality.



01 Thin stacked CMOS test die on a CMOS wafer



02 FIB-cross section of stacked CMOS test chips with 5µm diameter Cu TSV at 10µm pitch



03 3D-stacked test die with CuSn µbump connections

## MORE INFORMATION

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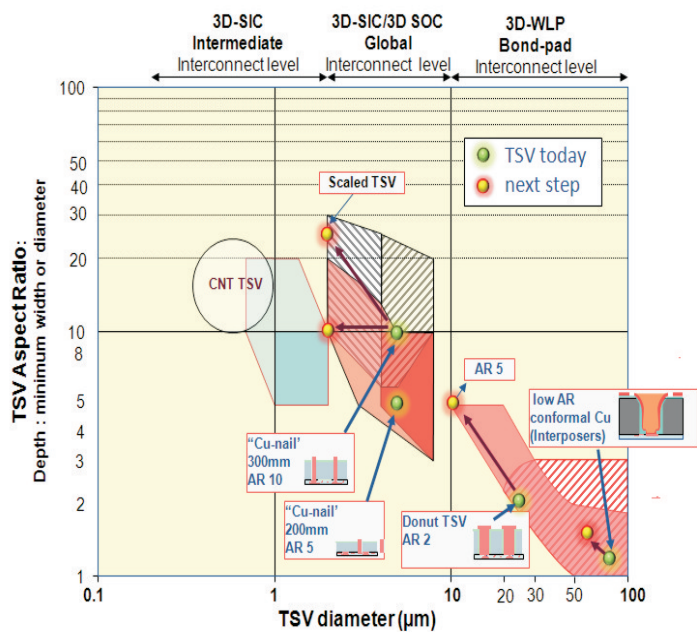
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## THE PROGRAM STRUCTURE

The program consists of tightly coupled technology and design sub-programs or activities. These 'horizontal' activities are strongly linked through the design, realization and characterization of test structures, which are organized as 'vertical' activities in the program.

## TECHNOLOGY

- ▶ 3D-TSV technology (3D-SIC and 3D-WLP)
- ▶ Wafer bonding to carriers, wafer thinning, backside wafer processing and wafer debonding and singulation
- ▶ 3D stacking and packaging technologies
- ▶ Technology characterization, modeling and reliability



Design: 3D SoC: Exploration of the impact of 3D technologies on system design for different 3D application domains:

- ▶ Path finding
- ▶ IP blocks for 3D integration: 3D memory, 3D-NOC
- ▶ Design for 3D integration
- ▶ Test strategies for 3D
- ▶ 3D System and Technology Cost modeling

Realization of active 3D test structures: vertical activity grouping the different subprograms:

- ▶ 3D logic-on-logic: 130nm CMOS (200 mm), and sub-65nm CMOS (300 mm)
- ▶ 3D DRAM-on-logic