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DATE Conference, booth F23, 13-16 March, Munich, Germany

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Treating low-k dielectrics for lower k values

By modifying the structure of the low-k material during or after patterning features in the low-k film, the dielectric constant can decrease compared to its as-deposited value.

Scaling the dielectric constant is one of the main driving forces for research and development of new back-end-of-line dielectrics. Whereas the scalability of the k value of spin-on materials was already demonstrated for some time and the porous spin-on low-k materials already appeared on the low-k dielectric roadmap for future generation, the scalability of the k value for CVD (chemical vapor deposition) dielectrics was so far uncertain. Experiments at IMEC have shown the feasibility that low-k materials can be treated for lower k values by penetration of etch or strip chemicals in the low-k material. The degree of penetration of the chemicals depends on pore size and properties of the chemical species. The lateral diffusion of the species is very fast in micropores, whereas the reaction with the low-k material itself is very slow com-

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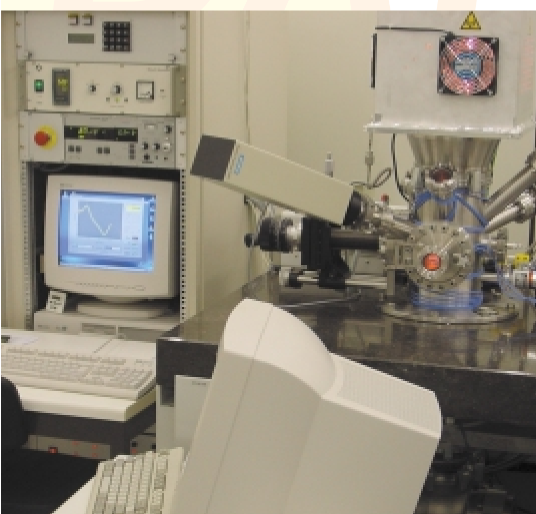

IMEC has developed a porosimetry measurement set-up based on adsorption ellipsometry, which has been used to characterize in detail density, free volume and interconnectivity of both porous and non-porous materials.

Platform design strategy for complex systems on FPGAs using OCAPI-xl

IMEC has developed a methodology to increase the granularity for the implementation of complex systems on FPGAs (field programmable gate array). The methodology has been applied on a JPEG encoder that will be used in a demonstrator of network reconfiguration.

Nowadays reconfigurable hardware like complex FPGAs has a fine-grain architecture that is generally not well suited for control-oriented applications. The control-oriented part is usually better mapped using a coarse-grain architecture like a processor. Mixed control/data applications, such as JPEG, also benefit from an increased granularity. A possible approach consists of a platform architecture that allows an efficient mapping of the system, using a coarse-grain architecture for the control path and a fine-grain architecture for the data path.

IMEC devised a novel methodology to exploit this concept. First, a system is partitioned in its data- and control-oriented tasks. The data-oriented tasks are mapped directly on the FPGA, while the con-

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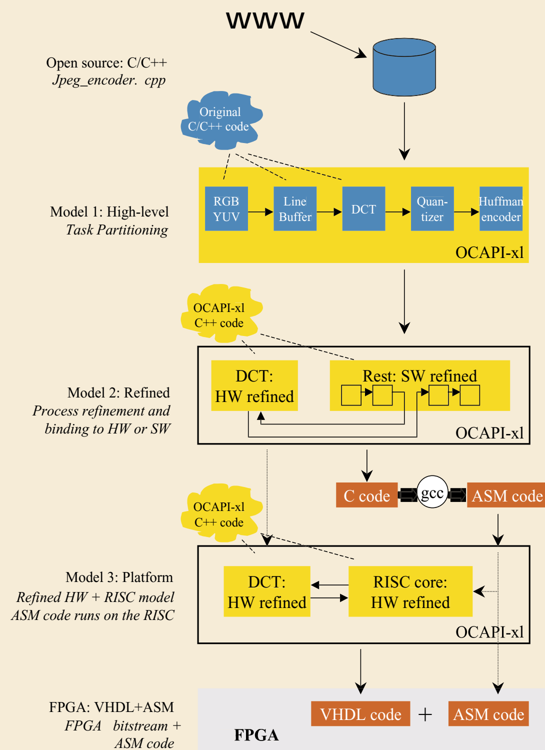

Design flow for JPEG encoder.

trol-oriented tasks are mapped on a processor. Since different parts of the system are implemented on architectures with different granularity, the underlying design environment must support the design on heterogeneous platforms. OCAPI-xl, the C++ library for system design developed at IMEC, is very suitable for this approach.

The design proceeds by constructing a model at a high level of abstraction and refining this model towards lower abstraction levels. Three levels can be identified. First, a high-level model expresses the functionality of the system. Secondly, the high-level model is refined. This refined model is expressed using the unified hardware/software modeling semantics provided by OCAPI-xl. It allows a fast exploration of the HW/SW boundary since no code rewrites have to be performed. Once the HW/SW partitioning is decided, code can be generated for both the

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software and the hardware parts. The third, platform-level model in OCAPI-xl consists of a model of the refined hardware part and of the processor used for the control-oriented tasks. The generated software is run on this model. This methodology encompasses the development of an OCAPI-xl model of the processor.

A JPEG encoder has been developed using this methodology. The data-oriented part of the JPEG algorithm, the DCT (discrete cosine transform), has been implemented in hardware, while the control-oriented part, the Huffman encoder, has been implemented in software. A 16-bit RISC softcore has been developed in OCAPI-xl together with a C compiler. It is implemented on the same FPGA as the hardware processes and is able to run the C code generated by OCAPI-xl. A high-speed instruction set simulator has also been developed, allowing third-party software development and acceleration of the co-simulation between the RISC core and the OCAPI-xl model of the system. For the JPEG algorithm, the three above-mentioned models were built. First, open source C code was partitioned in several processes. Next, these processes were refined and bound to hardware or software. Thirdly, the DCT model was co-simulated with the RISC model running the generated code for the Huffman encoder.

Further research in reconfiguration at IMEC focuses on mixed-design representations containing parts at different abstraction levels and their mapping on heterogeneous platforms containing a mixture of fine-grain and coarse-grain reconfigurable architectures.

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pared to the diffusion of the chemical species. However, the reaction takes place at each pore wall exposed to the chemicals. The very small reactions at pore walls can have a large effect on the overall k value, while the thickness of the low-k material remains substantially unchanged. To date, there is no good method available for lowering the k value of the as deposited film. However, experimental research at IMEC has shown that in-line processing appears to be a valuable option to lower the k value of the dielectric in narrow spacing for microporous materials, such as carbon doped glasses. Rather than protecting the existing material for possible degradation during further processing, the experiments concentrated on treating the films during patterning for lower k. Still, the details of the impact of the patterning process and Cu metallization on the dielectric properties need to be studied. The critical dimension of the microporous free volume, however, seems to be of key importance, since it will be responsible for the possible penetration of the treating medium and as such the enabling parameter for lowering the k-value.

It can be postulated therefore that both spin-on and CVD materials become an option for the k=2 dielectric families. Integration robustness and manufacturability as well as reliability will remain the parameters for decision making on the material of choice for integration.

Industry Link

IMEC's SoC++ design industrial affiliation program gains momentum

Three major semiconductor companies, including Infineon Technologies and STMicroelectronics, have joined IMEC's industrial affiliation program (IIAP) on object-oriented system-on-chip design.

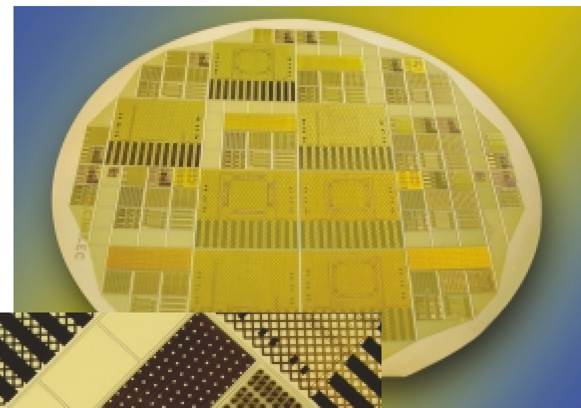
This IIAP targets the development of an application-domain specific design flow for systems-on-chip. Application domains include amongst others digital high-speed modems, multimedia systems, wireless local area network systems, networking components and systems, embedded protocol processing, embedded devices for mobile applications. The design flow is developed using object-oriented modeling in C++. The main outputs of the program are modeling libraries and design methods and tools that are specific to an application area, and refinement mechanisms that allow translating the models down to implementation level. Other tools can be used to perform advanced "what-if" analysis to explore system performance during the refinement process.
The IIAP continues the tradition of leading edge CAD research done at IMEC and targets system houses that want to develop a systematic design methodology for system-on-chip design both for hardware and software.

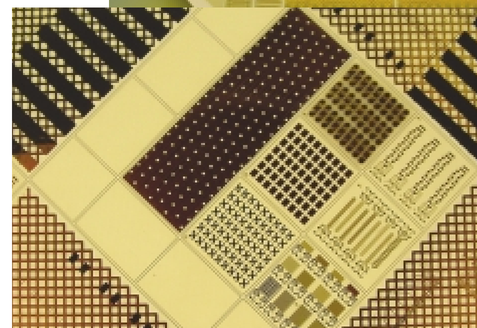
Technology report

High-density interconnection technology using thin-film on laminate

IMEC combines thin-film high-density interconnection capabilities with advanced build-up laminate board technologies.

Multi-layer thin-film technology (MCM-D) is generally accepted as the highest performance technology when it comes to achieving the highest interconnection density with the best electrical performance. The main features of IMEC's MCM-D technology are the use of copper for the interconnection lines, photo-sensitive benzocyclobutene (BCB) for the dielectric layers and electroless Ni:P/Au for the final contact metallization layer. Up to 5 metal layers are used. Furthermore, a resistor (20–200 Ohm/square) and a capacitor (0.6–1nF/mm²) layer may be integrated in the structure. The low processing temperatures also enable the use of a large variety of substrates.
These thin-film structures are generally produced on silicon, glass, ceramic or even metallic substrates, which only serves as carrier for the thin-film layers. After assembly of the die on such a substrate, the substrate itself needs to be packaged, increasing the overall system cost. This is an important disadvantage compared to laminate or ceramic high-density interconnect substrates, which can be considered as ball-grid-array "interposer" substrates, therefore not requiring any additional packaging, except for over-moulding and solder-ball attachment.





A promising IMEC alternative combines thin-film high-density interconnection capabilities with that of advanced build-up laminate board technologies. This so-called MCM-SL/D technology implements thin-film on top of a sequentially laminated printed circuit board. During the last year, significant progress was made in processing thin film copper and BCB layers on high Tg (glass transition temperature) laminate printed circuit board substrates, produced using a so-called sequential lamination of a double sided printed circuit board (PCB) and resin coated copper foils (RCC). Suitable PCB materials have been selected. A novel method for

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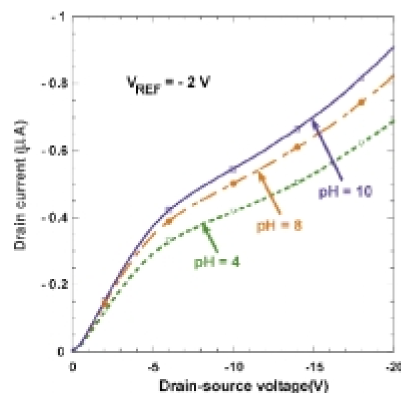
Polymer-based field-effect transistor for pH detection

Organic materials are good candidates for sensor technologies due to the simplicity of the fabrication process that lead to considerably lower costs compared to that of traditional semiconductor technologies. Within the main goal of developing low-cost (disposable) transducers for ionic charge detection, IMEC has fabricated and modified an organic-based field-effect transistor to achieve proton sensitivity. pH detection represents a generic principle which can be used for direct monitoring of proton concentration in body electrolytes as well as for the detection of neutral biochemical compounds (e.g. glucose, cholesterol etc.) when a layer of biomolecules with a specific recognition function (e.g. enzyme) is added to the transducer.

The detection principle is based on the field-enhanced conduction in an organic semiconductor (poly(3-hexylthiophene)). The electrochemical potential developed at the interface between the sample solution and the gate dielectric modulates the transconductance of the organic transistor.



Output characteristics of an organic-based transistor recorded in different pH buffer solutions (a bias VREF=-2V is applied on an Ag/AgCl electrode in respect to the source of the transistor)

Seven semiconductor companies joined IMEC's industrial affiliation program on wireless communication

Infineon Technologies and Sony recently joined IMEC's industrial affiliation program (IIAP) on integrated transceivers for broadband wireless multimedia communication. Today, the IIAP runs at full speed through the partnership with seven major semiconductor companies.

The objective of the program is to give partners early insight in algorithms and architectures for tomorrow's wireless multimedia communication. The driving application is an in-door wireless network that operates at multiple 100 Mbit/s. New algorithms and IP blocks are designed that will improve the system performance by several orders of magnitude. All parts of the system ranging from an optimized RF front-end over dedicated baseband digital processing to a protocol with quality of service provisions are taken into account.
The objective for the implementation of the RF front-end is a highly integrated single package solution, combining (Bi)CMOS IC integration for the active circuits and RF multi-chip module (MCM) technology for interconnection and integrated passives.
Research in baseband processing mainly focuses on modulation techniques with frequency domain processing such as OFDM. Moreover, novel algorithms are investigated to fully exploit spatial division multiple access, adaptive loading and turbo coding.
The final goal of this IIAP is to integrate a complete transceiver, consisting of an antenna, an RF front-end, a baseband processor and a protocol processor in a single package.

Digital circuits remain functional even after several hard breakdowns

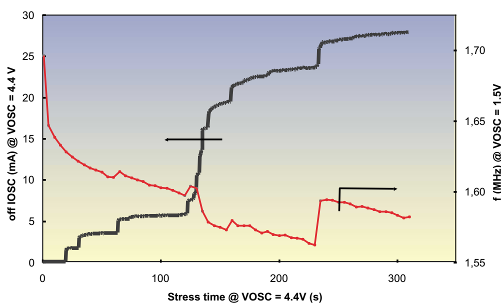
Reliability research at IMEC showed that some logical circuits remain functional even after several hard gate oxide breakdowns occurred in the circuit (presented at IEDM 2000).

A 41-stage unloaded ring oscillator with a 1:256 frequency divider with 0.18µm FET gate length and 2.38nm physical oxide thickness fabricated in 0.13µm technology has been investigated. After evaluating the basic static and dynamic characteristics at operating conditions (oscillator supply voltage V_{OSC}=1.5V), the circuit was statically stressed at V_{OSC}=4.4V for 5sec. The divider and buffer supply voltage remained at 1.5V. Afterwards, the circuit parameters were re-evaluated at operating conditions and the whole procedure was repeated.

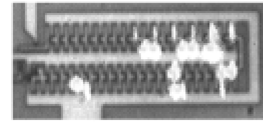
During the course of this experiment, the gate oxide in several transistors in the circuit broke down. The circuit, however, continued to oscillate, proving that every stage correctly transfers the logic information. It can therefore be concluded that even after multiple gate oxide breakdowns the circuit's logical function remains unaffected. The affected parameters include the frequency and the standby and dynamic supply currents.

To better understand the breakdown sequence, the circuit was stressed under an emission microscope and each jump in the oscillator supply current I_{OSC} was correlated with the appearance of new light-emission spots. The spots due to broken gate oxide and due to channel hot-electron emission could be identified by correlating the location of the spots with the positions of the stressed transistors and by spectral analysis. Channel-hot-electron stress develops due to voltage redistribution in the circuit in the vicinity of a broken transistor. "Satellite" breakdowns in adjacent transistors due to bipolar snapback are observed but are not expected to occur at operating conditions.

The circuit fails when a breakdown occurs in the frequency divider, suggesting that some parts of a digital circuit are more prone to a single FET breakdown. The researchers also concluded that a similar breakdown will most likely be fatal for an analog circuit. For digital circuits, however, the present reliability specifications constitute the extreme case as it was demonstrated that a non-zero probability exists that a digital circuit survives a FET gate breakdown. A more precise but more arduous projection of the circuit reliability will require finding the probabilities of all possible failure paths of the circuit. Based on this research, more reliable circuits could be designed by testing their susceptibility to gate oxide breakdown.



Although several transistors in the ring oscillator undergo gate oxide breakdown, observable as sudden increases in I_{OSC}, the circuit still oscillates.



Emission microscopy picture of the ring oscillator, showing the individual oxide breakdown spot and the corresponding satellite spots, caused by hot carrier generated light emission.

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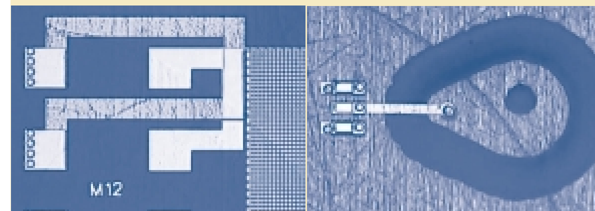
achieving a sufficiently flat starting surface for the thin film layers has been developed. This basically resulted in filling the gaps between the copper conductors and micro-via holes with a resin material, while achieving a local substrate flatness of ±5µm. By using first a thin film BCB layer on this substrate, a very smooth surface is obtained, well suited for applying



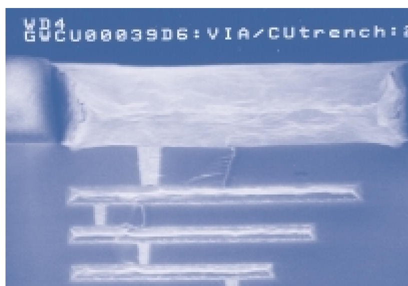
Photograph of a thin-film MCM-SL/D test pattern realized on a laminate substrate base. Left: meander pattern down to 10µm lines and spaces; Right: via pattern with 30µm via diameter and 20µm line width.

fine line thin film metallizations. With such an approach, electrical connections through the substrate may be realized and the substrate can be used as part of the MCM package, which can then be used as a ball grid array (BGA) style component.

Analog and RF functionality in an Aluminum back-end

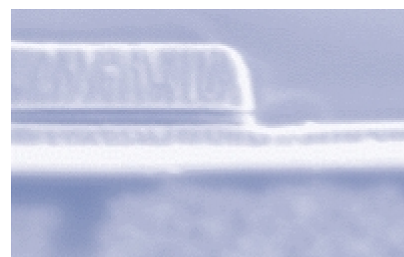
IMEC realized inductors with a high Q factor and high-precision capacitors in an Aluminum back-end for RF applications.

High-performance analog components with high Q factors in the GHz range are required for RF ICs in order to integrate as much functionality as possible on a single chip. Classic double poly capacitors and inductors fabricated in conventional back-end metal layers do not longer fulfill the needs for high Q factors and suffer too much from noise coupling from the substrate.
The substrate noise coupling of the inductor can be alleviated to some extend by using patterned shields. However, this technique also reduces the resonance frequency, which is not acceptable for many applications. Therefore, IMEC realized high Q inductors in an additional module using thick Cu metallization in a single damascene process on top of a classic three layers of metal Aluminum back-end. A Q factor of 24 at 2GHz was achieved on 20 Ohm.cm silicon substrates for an inductance value of 2.8nH.



SEM cross section of a 4µm thick Cu inductor with 2µm dielectric isolation to the top Aluminum layer.

Double poly capacitors can be optimized with respect to the stripe width of the top poly plate, in order to take full advantage of the silicide for series resistance reduction. This way, excellent Q factors could be achieved. However, the fabrication of the double poly capacitor on top of the field oxide inherently results in strong substrate noise coupling, even in presence of a junction isolated shield, such as a floating nwell. The fabrication of a linear capacitor on top of first or second metal layer strongly improves the dielectric isolation. Together with the low series resistance by using metal for both top and bottom electrode, a near ideal capacitor behavior is achieved over a frequency range up to 25GHz. An additional advantage is the relative low process complexity, which requires only one masking step. Due to the low topography in the back-end by using CMP (chemical mechanical polishing) for planarization, the capacitor matching is excellent with 0.3%µm for 1.1 fF/µm^2 capacitor density.



1.1 fF/mm^2 double metal capacitor.

IMEC's read-out ASIC for cosmic ray research in a successful balloon flight over Antarctica

IMEC developed a read-out ASIC for use with large arrays of silicon detectors in cosmic ray experiments. Last year, the ASICs have been mounted in an experiment set up for a balloon flight over Antarctica. The first balloon flew successfully for about 17 days.

In 1998, IMEC started a cooperation with NRL (Naval Research Laboratory) and NASA in Washington to develop an ASIC to read out the information from silicon detectors in cosmic ray experiments. The goal of the project was to investigate the source of cosmic rays in space. Astronomers have long thought that supernovas are the source of cosmic rays, but there's a troubling discrepancy between theory and measurements. To find out if the theory is in peril, a balloon was launched from Antarctica. The payload includes a NASA-funded cosmic ray spectrometer known by its builders as the Advanced Thin Ionization Calorimeter or "ATIC". ATIC is designed to measure the energy spectrum of

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Design, Automation & Test in Europe (DATE 2001) - special

IMEC presents at DATE its C++ based design technology for embedded systems, focusing on:

- Reconfigurable networked appliances;
- C++ for hardware/software refinement;
- Memory optimization;
- Mixed-signal design.

IMEC will demonstrate at DATE:

- Networked reconfiguration enables flexible Internet camera
- OCAPI-xl: unified modeling and refinement of HW and SW
- Low-power pre-compilation of multimedia applications on programmable processors
- ATOMIUM/MemoryCompaction: automated memory size reduction for multimedia applications
- Co-simulation of digital modem with RF front-end by coupling FAST and OCAPI-xl
- Experimental verification of noise coupling analysis with SWAN

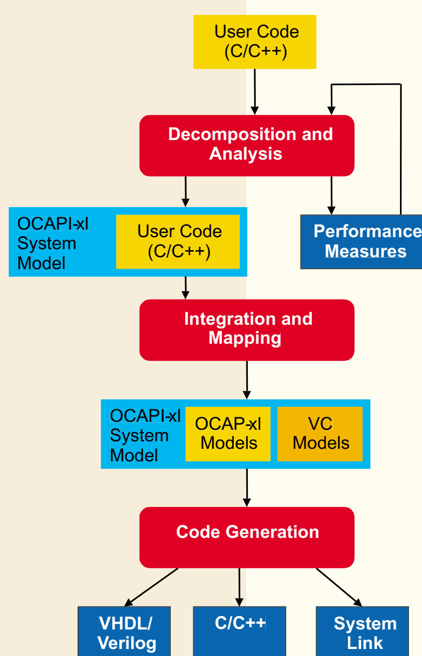
Reconfigurable networked appliances

Networked reconfiguration enables flexible Internet camera

During the DATE exhibition, IMEC will demonstrate a web-serving camera that was built on a reconfigurable platform. At the heart of the platform is a Xilinx Virtex FPGA. The FPGA supports high-throughput image formatting and GIF encoding of data, read from a CMOS image sensor. Network connectivity is established through a standard 10 Base-T Ethernet connection.
The camera can be directly accessed from a web browser client on the same network. The client can receive live images, and can also perform distant programming of the camera. This includes a wide range of tasks, from changing image parameters up to online reprogramming the FPGA content and consequently the camera function.
The camera platform was entirely designed in OCAPI-xl, an in-house developed C++ based digital system design environment.

C++ for hardware/software refinement

OCAPI-xl: unified modeling and refinement of HW and SW



Design flow supported by OCAPI-xl.

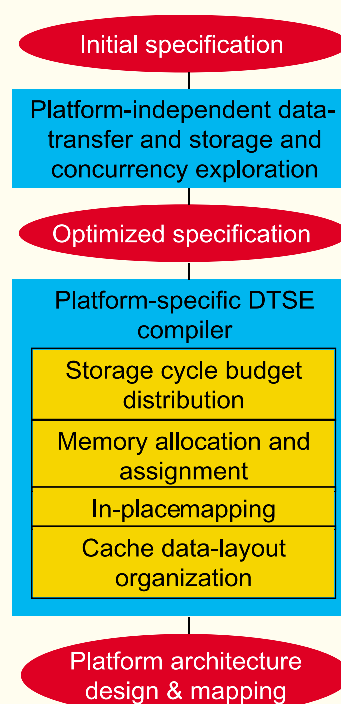
OCAPI-xl is a C++ library for analysis, refinement and mapping of tasks on digital platforms. It is a second generation C++ based design environment that evolved out of OCAPI-1 and earlier design experiences with C++ based design.
A major improvement in OCAPI-xl is that it effectively allows a single representation from which both synthesizable HDL and embedded software can be generated. This enables a novel and more effective design method when targeting large fine-grain reconfigurable platforms.
At DATE, IMEC will demonstrate a JPEG image encoder that is refined to a mixed hardware/software implementation. The exploration model is a multi-process description and uses OCAPI-xl modeling semantics. The refinement tasks elaborate the local computation and system-level communication aspects, and create a refined OCAPI-xl C++ model. Part of this model is then automatically converted to HDL suitable for FPGA and part to C code suitable for an embedded core.
The demonstration shows a development environment consisting of the OCAPI-xl library and a small RISC core with C compiler support that can be mapped on the FPGA. The RISC core was also developed with OCAPI-xl.

Read more on this topic: page 1

Multimedia systems typically require a very large amount of data storage and transfers, which causes high system costs. IMEC has developed a data transfer and storage exploration methodology to globally optimize the memory accesses, leading to better CPU performance, low system bus load and a low-power realization. The use of this methodology on real-life multimedia applications has resulted in a speed-up of up to a factor 3, a typical reduction in memory bus load (on-chip and off-chip) with an order of magnitude, and a significant energy consumption reduction. At DATE, IMEC will present both its research on data transfer and storage exploration (DTSE) focused on predefined and programmable architectures, and its ATOMIUM CAD environment that assists designers in applying the DTSE methodology for custom architectures.

Low-power pre-compilation of multimedia applications on programmable processors

The DTSE optimization methodology is complementary to traditional compilers. It consists of platform-independent steps in the initial stage encompassing data transfer, storage and concurrency exploration. The optimized specification resulting from this stage is used as input to the various platform-dependent steps. Storage cycle budget distribution aims at reducing memory bandwidth and bus load. Memory allocation and assignment guarantee a cost efficient memory architecture. In-place data mapping (see ATOMIUM/Memroy-Compaction) reduces memory capacity requirements but also capacity and compulsory cache misses apart from reducing write backs to the main memory. Finally, a new main memory data layout organization technique is applied to remove the majority of conflict cache misses.



Systematic DTSE methodology for (parallel) programmable multimedia platforms. Note the platform-independent steps in the initial stage and the subsequent platform-dependent steps.

ATOMIUM/MemoryCompaction: automated memory size reduction for multimedia applications

The ATOMIUM toolbox is a CAD environment that assists the designer in analyzing and optimizing data-dominated systems at a high level. ATOMIUM operates at the behavioral level of an application, expressed in C. The output of the environment is a transformed C description, functionally equivalent to the original one, but typically leading to strongly reduced memory size and power consumption. The latest addition to the toolbox is a tool called “MemoryCompaction” that aims to maximize the reuse of memory locations, hence reducing the required memory size and power consumption for the application. To this end, the tool automatically optimizes the storage order of multi-dimensional data. In a first optimization phase, intra-data storage order optimization, the tool searches for an optimal order and direction for the dimensions of each multi-dimensional data structure separately, with the goal of reusing memory locations as much as possible inside each data structure. The aim is to find a minimal address reference window for each data structure. This window is used to fold the address ranges (through a modulo operation). In the second phase, the inter-data storage order is optimized. Based on a geometrical global life-time analysis, the tool

places the data structures in the memories such that locations are reused as much as possible between different data structures. Finally, when the user is satisfied with the results, the tool can apply the necessary transformations to the source code. This is done by combining the multi-dimensional index expressions, found in the code, with the obtained storage orders into one-dimensional address expressions.

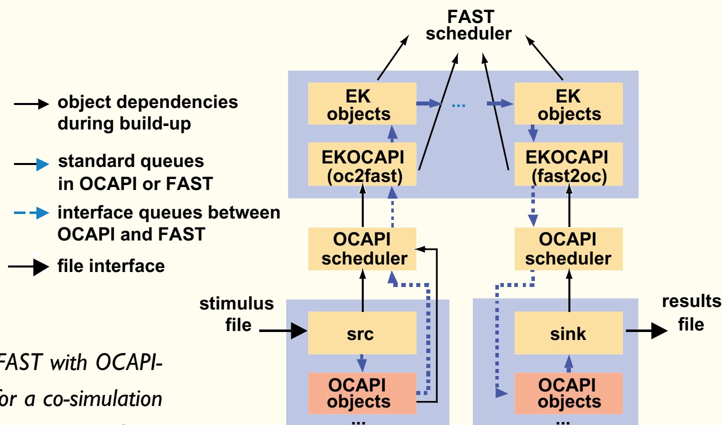
Mixed-signal design

Cost-effective implementation of wireless transceivers compels a small size and low power consumption and thus implies a high degree of integration, combining analog and digital functions. This requires development and thorough analysis of new front-end architectures, an activity that must be supported by simulations at the architectural level. To this purpose, IMEC uses the combination of two in-house developed tools: OCAPI-xl, a digital modeling and simulation environment, and FAST, a simulator for RF front-end architectures. At DATE, IMEC will show an efficient high-level simulation of a mixed-signal 5GHz WLAN (wireless local area network) transceiver by coupling FAST and OCAPI-xl.

In mixed-signal ICs the switching noise generated by the digital circuits propagates through the substrate of the IC and disturbs the analog circuitry. The program SWAN, developed at IMEC, provides analysis of this substrate noise in mixed-signal ICs of practical size and will be demonstrated at the DATE exhibition.

Co-simulation of digital modem with RF front-end by coupling FAST and OCAPI-xl

Wireless transceivers with a high degree of integration and low power consumption require careful co-design of the digital modem with the analog front-end. To support such co-design, IMEC couples two in-house developed tools: OCAPI-xl, a digital modeling and simulation environment, and FAST, a simulator for RF front-end architectures. Since FAST is in essence a dataflow simulator it can be relatively easily coupled with the dataflow simulation module of OCAPI-xl. The communication between the two programs is via FIFO buffers.

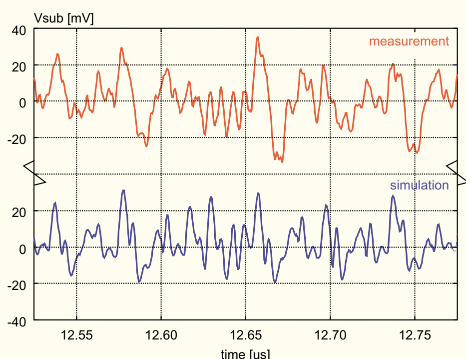


Coupling of FAST with OCAPI-xl: scenario for a co-simulation of the digital transmit and receive parts with the RF front-end of a wireless transceiver.

The coupling of FAST and OCAPI-xl has several advantages. FAST is a very efficient simulation engine that minimizes the simulation overhead of taking into account the analog blocks during simulations of a complete telecom link. Moreover, accurate high-level simulations require accurate models for the different transceiver blocks, which are delivered by the program DISHARMONY, also developed at IMEC. DISHARMONY generates high-level models for analog front-end blocks such as amplifiers (e.g. low-noise amplifier, variable-gain amplifier) and active filters, starting from a circuit netlist. The models take into account the frequency dependence of the non-linear behavior of the circuits. For the digital blocks, the OCAPI-xl environment further provides a path from the dataflow level down to VHDL or Verilog.

Experimental verification of noise coupling analysis with SWAN

The SWAN methodology enables efficient and accurate simulations of the substrate noise generated by large digital circuits. Hereby, the two major sources of substrate noise are taken into account: noise coupling from the switching gates and noise coupling through the power supply lines. The dominant noise source is determined by the package parasitics, such as bondwire and pin inductance, which are causing the noise on the power supply.



Comparison of simulated and measured substrate noise on an 86Kgate digital ASIC.

The methodology consists of two parts: standard cell library characterization and substrate noise waveform computation. First, the substrate noise generation and power supply current consumption of all standard cells, as function of the switching activity of the cell, are extracted together with a macro-model of the substrate of the cell. This step has only to be done once for a given technology. Next, for a given digital design all switching events of each gate are extracted from a standard gate-level VHDL simulation. By combining the noise generation of each gate with the switching activity data, an accurate waveform of the substrate noise voltage is calculated in a simulation time of the same order of magnitude as the digital gate-level simulation time.
Recently, simulation results from SWAN have been verified with measurements on an 86Kgate digital ASIC (presented at ISSCC 2001). The difference in simulated and measured substrate voltage RMS value is less than 10%.

Attend the DATE Telecom day on Thursday 15 March 2001

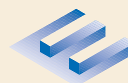
DATE 2001 features a special day focused on current issues in telecom design. The telecom day, co-organized by IMEC, will be the place for exchanging telecom design experiences with colleagues, for picking up new ideas on how to design telecom systems and to see the latest telecom design tools.
The embedded tutorial during this day, in which IMEC will give a presentation, will be devoted to efficient and accurate simulation of integrated RF circuits and systems. Also a complete technical session will be devoted to simulation of RF systems. IMEC researchers, for instance, will present a new and efficient method for simulating bit-error-rates of multi-carrier transceivers.

Visit DSP Valley at DATE, booth # F231

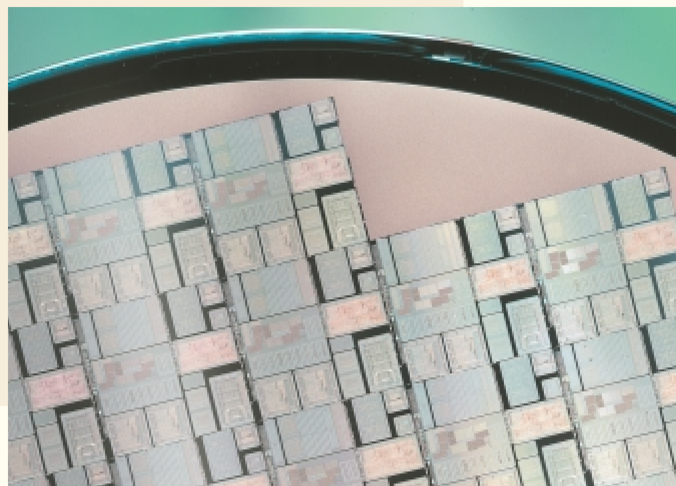
IMEC is member of DSP Valley, a technology network organization, focusing on the design of hardware and software technology for digital signal processing systems. DSP Valley groups members of different kinds: universities, research institutes and industrial companies.

Visit Europractice at DATE, booth # A3

The EUROPRACTICE IC Service, coordinated by IMEC, offers low-cost ASIC prototyping and ASIC small volume production through multi project chip (MPC) and dedicated wafer runs.



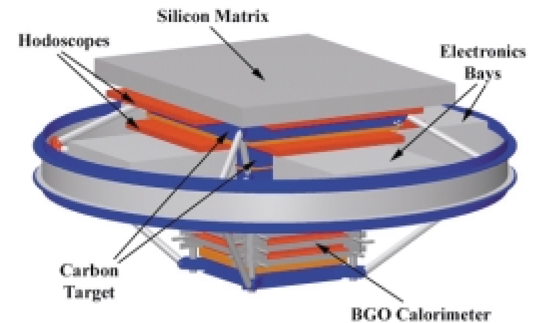
EUROPRACTICE
IC SERVICE



continued from p.6

individual cosmic ray elements in order to study the validity of the theory.
The instrument is based on the technique of ionization calorimetry, the most practical method of energy determination for cosmic ray nuclei from H to Fe over the target energy range (50 GeV to >100 TeV). The silicon matrix detector provides an accurate measure of the incident particle charge. It consists of 4480 separate detector pads that are separately read out using an ASIC, which was designed by IMEC. The ASIC provides 16 channels of front-end electronics for integrating the charge pulses from the silicon detectors and presents the results as a held DC level. The 16 channels are multiplexed to a common output buffer on the chip. The noise of the chip is low enough (~4000 electrons rms for a detector capacitance of 100pF) to clearly distinguish minimum ionizing proton signals while the dynamic range is sufficient to measure charges from H to Fe even at large incidence angels. The chip was designed in the 2.4µm CMOS technology of Alcatel Microelectronics and the nominal power consumption is <5.5mW/channel.

Layout of the ATIC read-out ASIC



The ATIC balloon payload and schematic of the instrument.

Industry link

Infineon Technologies has extended semiconductor research work with IMEC

Infineon Technologies has extended its collaboration with IMEC in the field of microelectronics technology and design- and system-oriented research.

Infineon, which has a longstanding relationship with IMEC, has joined several IMEC Industrial Affiliation Programs (IIAPs). The organizations will collaborate on advanced CMOS process steps and modules, which will focus on providing basic technologies for manufacture at dimensions of 70nm or less, and advanced optical lithography. Additional joint activities cover system-on-chip (SoC) design and wireless local-area networks (WLANs) system applications.
The cooperation on process technology will address critical CMOS technology process developments. The research program on high-k gates aims to develop gate dielectrics and gate electrodes for (sub)-100nm devices. Research will also be performed on interconnection technologies based on the use of low-k materials and Cu. Another part of the cooperation targets the optimization of silicide processing aspects and shallow junction formation for industrial processes.
Finally, Infineon and IMEC will jointly develop optimized cleaning strategies and novel cleaning concepts.
The organizations will also collaborate in a joint lithography program that aims at extending the limit of optical lithography into the sub-100nm region. The program will focus on research of very deep UV-lithography processes with 157nm optical wavelength.
To support the industry's movement to SoC solutions, which requires more functionality to be added to mainstream digital CMOS at acceptable cost levels, flash

continued next page

memory embedded as a processing module in state-of-the-art CMOS has become a very competitive technology. Infineon and IMEC will cooperate to extend the company's expertise in embedded non-volatile memories into the deep-submicron regime. Heart of the cooperation is an advanced flash development program which covers scaling issues of flash memory cells and technology, reliability issues related to scaled flash memory technologies, and advanced concepts.
The SoC trend also places greater demand on design methodologies, including hardware/software co-design. Infineon has joined collaboration with IMEC on application-domain specific design flows using object-oriented modeling in C++. The first application domain targeted is broadband wireless communication. In addition Infineon entered IMEC's system design program for wireless local area network solutions.

MEMS design and technology agreement with INTI-CITEI, Argentina

IMEC has signed a two-year agreement with INTI-CITEI, the Argentinean research center for telecommunications, electronics and information technology. The agreement allows INTI to use IMEC's technology and design know-how of micro-electromechanical systems (MEMS) and advanced packaging technology for internal R&D purposes.

Signing of the technology agreement between IMEC and INTI-CITEI at the presidential palace of Buenos Aires

INTI-CITEI is engaged in the business of thick-film technology and plans to upgrade its current facilities, to set up a state-of-the-art MEMS laboratory. The acquisition of IMEC's packaging and MEMS technologies is a first step towards the introduction of highly advanced microelectronics into Argentinean industry and, more specifically, into specialized small- and medium-sized enterprises. INTI-CITEI also plans to introduce these advanced technologies after two years into the other member states of the MERCOSUR countries (Argentina, Brazil, Uruguay, Paraguay and Chile).
This agreement is of significant importance for IMEC, as it increasingly widens its industrial activities to play a worldwide role in the industrial development of microelectronics. The contract enables IMEC to introduce its existing research and know-how in various fields of microelectronics, as well as its highly advanced training programs, to the Latin-American continent, and more specifically to the MERCOSUR member countries.
This agreement is the next phase in a collaboration following the Memorandum of Understanding between an Argentinean delegation and IMEC, signed on April 20, 1999, during the Flanders Technology Fair in Ghent (Belgium).
The Memorandum of Understanding provided for the establishment of a joint working group to determine the feasibility of a new microelectronics center in Argentina. Since that time, discussions have been held between IMEC and INTI on the technical, financial and IPR (intellectual property ruling) aspects of the new microelectronics center.

Germany based Micronas GmbH licenses 0.25µm CMOS technology from IMEC

IMEC has licensed its 0.25µm CMOS technology to Micronas GmbH. This 0.25µm CMOS technology includes both the standard digital CMOS as well as the analog modules including double poly devices. This high-performance CMOS technology employs STI (shallow trench isolation) for device isolation, $CoSi_2$ salicided schemes, thin-gate dielectrics and nitride spacers. The backend is an Al- and W-plug based full CMP (chemical-mechanical polishing) multilevel technology.
This 0.25µm technology will be the next technology for the future generation high performance full-custom mixed-signal products of Micronas manufactured at Freiburg. Target application areas are high-performance consumer audio and video, multimedia as well as automotive.

IMEC and Sony signed research collaboration programs on fundamental technologies for next-generation semiconductor systems and devices

IMEC and Sony Corporation have signed a research collaboration program in the areas of wireless local area network (WLAN) and bipolar CMOS process technology.

The growing market pressure for high-performance semiconductors compels the industry to introduce new technologies at an unprecedented speed. This, together with intensifying technological challenges, can generate enormous investments in R&D, which necessitates global collaboration efforts between companies, independent laboratories and academia. In light of this, IMEC launched industrial affiliation programs (IIAP) in which companies from all over the world participate to jointly develop next-generation semiconductor technologies on the basis of cost sharing and risk reduction.

In the area of broadband WLAN, Sony will participate in the IIAP to attain IMEC's advanced system know-how and designing/modeling methodologies for 5GHz WLAN solutions. Results of the collaboration will be transferred to Sony to facilitate the development of its proprietary WLAN device solution for future wireless consumer electronic products. Sony's engineers will participate in the IIAP as resident researchers for a period of two years.

In addition to the IIAP, the two companies agreed to enter into a technology transfer program, in which modules of IMEC's bipolar CMOS process technology will be transferred to Sony. Bipolar CMOS technology will foster the development of high-speed analog ICs that will become necessary to process high frequency signals for next-generation consumer electronic products in the broadband network era.

STMicroelectronics and IMEC jointly develop low-power design methodology and tools

STMicroelectronics has entered IMEC's industrial affiliation program on object-oriented system-on-chip design for joint research into the development of low-power design methodology and tools.

Under this agreement parts of the tools for DTSE (data transfer and storage exploration) will be developed at IMEC by a team of STMicrolectronics residents and IMEC researchers. DTSE pioneered at IMEC to reduce the power consumption of applications running on embedded processors. It is a methodology and a tool-chain for transforming an application code written in C/C++ language to an optimized code, which while retaining the original functionality, compiles to a more power efficient firmware.

Sections of the tools have already been developed, tested and their potential verified over the past ten years at IMEC. However, to complete the process so that the methodology can be put into practice by application developers in an easy-to-use environment, more research and development is required. Sections of the methodology, which are difficult and laborious to apply manually, are the prime targets of automation through tools.

Calendar

EUROSIME conference - April 9-11, 2001, Paris, France

2001 International symposium on VLSI technology, systems and applications (2001 VLSI-TSA)
April 18-20, 2001, Taiwan

International workshop on information processing in cells and tissues (IPCAT'2001)
August 13-17, 2001, Leuven, Belgium

For more information: http://www.imec.be/6/6.html

SENSOR 2001

8-10 May 2001, Nürnberg, Germany

Booth #2-216

SENSOR, known as the world's biggest fair for sensors, processing electronics, system solutions and related services, will take place in 2001 for the tenth time. The broad and technologically concentrated spectrum of this trade fair ranges from the electrical and electronic industry to the diverse engineering branches, from consumer industry to automation technologies and the automobile industry.
IMEC will exhibit at SENSOR 2001 and present its advanced sensor technology focusing on infrared, imaging and biochemical sensors. Visit IMEC at booth # 2-216 and learn more about its development of complete biosensor systems based on the unique integration of microelectronics and biotechnology for the demonstration of novel applications for monitoring, protecting or improving human health.
Together with its spin-off XenICs, which develops and markets innovative infrared image sensors, IMEC will demonstrate a linear infrared sensor for wavelength division multiplexing applications (1.7μ) and infrared (2.5μ) spectroscopic sensing. The hybrid infrared sensors combine InGaAs arrays with CMOS read-out circuitry.
At the same booth, IMEC's spin-off FillFactory, which develops and commercializes high-performance CMOS image sensors, will present demonstrations based on CMOS imaging technology showing both the integrating IBIS and the logarithmic FUGA sensors.

For more information:
http://www.imec.be/sensor/

38th Design Automation Conference

18-20 June 2001, Las Vegas, USA

Booth # 1133

The Design Automation Conference (DAC) is the premier electronic design automation (EDA) and silicon solution event. DAC features an outstanding technical conference with over 50 sessions led by leading system designers and researchers presenting the latest in design methodologies and EDA tool developments along with industry trends and information.
IMEC will exhibit at DAC in the Convention Center. Visit us at booth # 1133 where you can attend our life demonstrations and learn more about IMEC's core competence in design technology for systems-on-chip.
For more information:
http://www.imec.be/DAC/

SEMICON West 2001 – Semiconductor processing and wafer fabrication

16-18 July 2001, San-Francisco, USA

Booth # 4417

SEMICON West is the largest international exposition and conference dedicated to semiconductor equipment, materials and services in the world. Each year, more than 50,000 semiconductor professionals converge upon SEMICON West to network and exchange ideas and information on new and emerging products and technology. SEMICON West 2000 will feature technical programs and sessions on the most critical challenges facing semiconductor manufacturers.
IMEC will exhibit at SEMICON West in Moscone Center, Esplanade Hall.
Come to visit us at booth # 4417 and talk to IMEC's president & vice presidents, research directors, sub-micron pilot line experts, ... about IMEC's R&D activities, research strategy, new training initiatives, sub-micron process technologies transfers from IMEC to companies worldwide, IMEC's Industrial Affiliation Programs, …

For more information:
http://www.imec.be/semiconwest/

Training program 2001

MTC

Calendar

Design of experiments – introductory 4 days course
Session 1: 15/02, 27-28/02, 12/03
Session 2: 15/03, 21-22/03, 03/04
Session 3: 04/05, 14-15/05, 23/05
Session 4: 26/06, 03-04/07, 10/07
Session 5: 04/09, 11-12/09, 24/09
Follow-on day: 30/04

Artificial intelligence with Europace: 5 seminars
21/02, 07/03, 28/03, 18/04, 09/05

A unified meta-flow - The grandmother of all system design flows 01/03

Perl 3 days course: 05-06/04 & 09/04, 10-12/04

How to write code for high-performance low-power multimedia applications?
4 days course: 07-10/05, 17-20/09, 10-13/12

Address optimization
1 day course: 11/05, 21/09, 14/12

ASIC design and manufacturing flow for managers: introduction to integrated circuit technology
14/05

How to write VHDL and efficiently synthesize your circuits? 5 days course: 28/05 – 01/06

Silicon processing for ULSI fabrication
5 days course: 01-05/10

For more information: http://www.imec.be/mtc/

Patents

US

Etching of $CoSi_2$ in HF-based solutions (US 6153484)
A spatially-modulated detector for electromagnetic radiation (US 6157035)
A method of erasing and a method of programming a memory device for low-voltage and low-power applications and a new memory device (US 6144586)
A method for measuring electromigration-induced resistance changes (US 6136619)
Gastro-intestinal Probe (US 6006121)
Metal rinsing process with controlled metal microcorrosion reduction (US 6153018)
An imager or particle detector and method of manufacturing the same (US6121622)
A device for emitting electromagnetic radiation at a predetermined wavelength and a method of producing such device (US 09070455)

Korea

Transistor structure for erasable and programmable semiconductor memory device (KR 280051)

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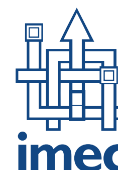

nº 29 March 2001 imec newsletter

I want to receive more information on:

- ❑ Treating low-k dielectrics for lower k values
- ❑ Digital circuits remain functional even after several hard breakdowns
- ❑ Thin-film high-density interconnection on laminate
- ❑ OCAPI-xl design environment
- ❑ Memory optimization for multimedia applications
- ❑ Mixed-signal simulation
- ❑ Other: ....

Please put me (or my colleague) on your mailing list for following publications:

❑ IMEC scientific report ❑ IMEC annual report ❑ IMEC newsletter

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