



Years of Making
Technology Fly

NEWSLETTER

55
JANUARY 2009

NEWS
FLASH

IMEC and Panasonic sign comprehensive joint research contract

Cutting-edge CMOS processes and More than Moore research (networks, wireless, and biomedical)

IMEC and Panasonic Corporation have signed a joint research contract concerning the most advanced technologies in the semiconductor, networks, wireless, and biomedical fields. Research will be carried out at the Leuven (Belgium) facilities and at IMEC's research unit at Holst Centre in Eindhoven (the Netherlands).

Since 2004, Panasonic has been participating in IMEC's joint research platform on the most advanced semiconductor process technologies as a core partner to accelerate its open innovation in this field.

The world's first mass production of the system-on-chip with 65nm and 45nm processes such as Panasonic's 'UniPhier[®]' uses the results of the joint research with IMEC. Now, a comprehensive joint

research program covering most of the research domains of IMEC will start by expanding the collaboration scope from advanced semiconductor process technology to include application areas of semiconductors.

For this purpose, the Panasonic IMEC Center has been established at the IMEC premises in December 2008. It will conduct R&D on network technology such as dynamically reconfigurable software-defined radio, ultra-low power consumption wireless

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News from IMEC's CMORE platform

NEWS
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IMEC builds reliable 11 megapixel micro-mirror array for high-end industrial applications

At the IEEE International Electron Devices Meeting 2008, IMEC presents a monolithically integrated 11 megapixel micro-mirror array for high-end industrial applications, a world's first both in terms of pixel density and reliability. Each mirror in the array is $8\mu\text{m} \times 8\mu\text{m}$ and can be individually tilted by the high-speed integrated CMOS circuitry underneath the array. This device fits in IMEC's CMORE initiative, which offers cost-effective solutions for continued system scaling, not by shrinking CMOS but by focusing on monolithic co-integration of heterogeneous technology.

IMEC's 10cm^2 11 megapixel mirror array has a pixel density that is almost double that of comparable state-of-the-art micro-mirrors. And IMEC has demonstrated that its mirrors show no creep and

remain reliable for at least 2.5×10^{12} cycles. Integrated micro-mirror arrays, such as this one, are used in, for example, video projection or lithography mask writers. IMEC fabricated the $8\mu\text{m}$ mirrors on top of foundry

high-voltage $0.18\mu\text{m}$ CMOS 200mm wafers with 6 interconnect levels. The array was built using IMEC's proprietary SiGe-based MEMS platform, meeting the mirror's mechanical reliability requirements, device flatness, and compatibility with high-speed CMOS. Poly-SiGe was chosen as structural material for the mirrors, instead of Al. Poly-SiGe solves many of the reliability issues of Al-based mirrors, and it is compatible with above CMOS processing, allowing a smooth integration with the CMOS chip below.

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Editorial



On January 16, 1984 the memorandum of association of IMEC as a non profit organization with a mission to do research in microelectronics was signed. At that time, no one could have expected that, 25 years later, it would grow into a world-renowned institute. But it was recognized that the new organization had potential and that it could contribute to the microelectronics sector, to industry and also to society at large. One thing is for sure: IMEC developed into a famous institute, due largely to the vision of its founders, to the leadership of Professor Baron Roger Van Overstraeten, who would look back proudly to his life-dream, to the continuity of policy and cooperation with the government of Flanders, governmental institutes and Flemish universities, and most of all to the enthusiasm of its employees. The perfect combination of people who have built up years of knowledge and experience at IMEC and the continuous inflow of young talent from all over the world, was and still is a pre-requisite for doing top-level research. Together, we succeeded in putting Flanders on the world map of micro- and nanoelectronics.

Predicting the next 25 years is difficult. IMEC is nonetheless ready to tackle the challenges of the nanoelectronics era. Together with the leading semiconductor companies, we will certainly continue to scale CMOS technology. More and more attention will be paid to adding extra functionality on chips. We also feel that the momentum is building to expand the other research areas in which we are active, areas such as solar cell technology, biomedical electronics and photonics. That way, IMEC will contribute to Flanders, Europe and the world of tomorrow, where centers of excellence will play an important role.

To celebrate the happy occasion of IMEC's 25th year, we will organize a host of events, such as the academic session on April 2nd. Do not miss the IMEC Technology Forum 2009 on June 3 and 4 in Brussels, the successor of IMEC's Annual Research Review Meeting. Over the years, ARRМ has evolved into a true industry networking event where you get first insights into the potential of technological innovations. The IMEC Technology Forum, which focuses on open innovation, looks ahead to the future of nanoelectronics and gives you inspiring ideas on future applications ranging from energy, communication, and biomedical electronics to the intangible.

I wish you a fruitful and interesting new year and I hope you will join us to celebrate this festive 2009!

Gilbert Declerck, President and CEO IMEC

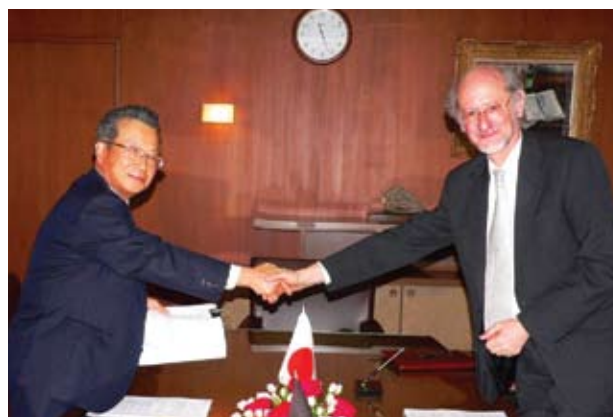
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IMEC and Panasonic sign comprehensive joint research contract

communication technology for healthcare and lifestyle monitoring and bio-medical technology such as next-generation biosensors.

Recently, thanks to the evolution of systems-on-chip, consumer electronics have advanced with higher performance, smaller size and lower power consumption. Future evolution of semiconductor technologies and integration with various other technologies is expected to further broaden application domains. In order to accelerate such evolution and integration of different technologies, joint research among the world class research institutes is essential.

Panasonic is enhancing its R&D in networks, healthcare devices and semiconductor technologies to realize an environmentally-friendly ubiquitous networked society. Panasonic will make further acceleration of R&D on cutting-edge technologies by expanding the scheme of joint research with IMEC, the world outstanding nanoelectronics research center as well as the world-leading research center in applications of semiconductor technology.



Dr. Susume KOIKE, Executive Vice-President Panasonic Corporation, and Prof. Gilbert Deckerck, President and CEO IMEC, shake hands after sealing their agreement for an extended collaboration.

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First direct imaging of oscillating microbubbles in a megasonic wafer cleaning system

In-depth look into microscopic effects in megasonic cleaning

IMEC, in collaboration with the Physics of Fluids group at the University of Twente (the Netherlands), has for the first time visualized the dynamic behavior of microbubbles that play a central role in megasonic cleaning. This in-situ imaging will contribute to a better understanding and, eventually, to a better control of the megasonic cleaning mechanism, which is considered an important technology for the removal of contaminants and nanoparticles of future device generations.

In future generation devices, the amount of surface etching that can be tolerated is so small that pure chemical cleaning will be insufficient to obtain a significant particle removal effect. Therefore, a mechanical component needs to be added to the cleaning process. The use of MHz-range acoustic agitation has been widely applied since many years. Yet it is found that with state-of-the-art cleaning technology, the fine patterns on the wafer surface are significantly damaged. Since alternative techniques suffer from similar issues, it seems that the cleaning technology is hitting a wall. Even megasonic technology that has been implemented for a long time turns out to be poorly controlled. What is more, the exact cleaning mechanism is not well understood and is subject to debate.

At IMEC a comprehensive program has been set up to tackle this issue. This program includes a strategic collaboration with the Physics of Fluids group at the University of Twente, which is a center of excellence in micro-fluidics. The activity concentrates

on the microscopic level. In acoustically agitated liquids, microscopic cavitation bubbles are created. It is expected that the dynamic behavior of these microbubbles plays an active role in megasonic cleaning. The focus of this study is to better control this microbubble dynamics in order to maximize the removal of particles while avoiding the generation of damage to fine patterns. At this point, more understanding is built up through in-situ visualization of both the removal of nanoparticles and the sub-microsecond timescale dynamics of the cavitation bubbles responsible for this removal.

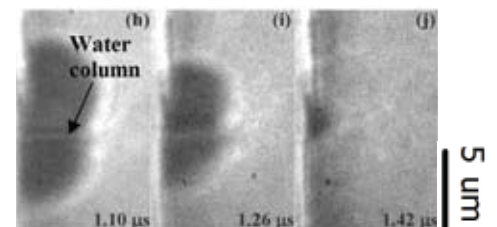
To capture the sub-microsecond timescale dynamics of these bubbles while cleaning the substrate, recordings were made using an ultra-high-speed camera named Brandaris, at a frame rate around 14 million frames per second.

Microbubbles were observed that strongly oscillate with the 1MHz driving sound pressure cycles. A movie has been made of a strongly oscillating hemispherical microbubble observed in side-view

on the edge of the glass substrate, with a maximum base diameter of about 10µm. The bubble shows a remarkably strong response to the driving sound field. One can see that it strongly changes in size, and, taking into account the instrumental resolution limitations, the bubble is believed to collapse completely. Due to the presence of the substrate, the collapse occurs in an 'asymmetric' way.

In future work, emphasis will be on the relation between individual bubble activity and local particle removal effects and potential damage formation on a microscale. Finding out the behavior and determining the main parameters are believed to provide the key to a better controlled process.

Side view of a microbubble on a substrate in a 1MHz acoustic sound field in water obtained with an ultra-high-speed camera at 14 million frames per second. The 3 selected frames with an interframe time of 79ns show the fast collapse of the bubble.



These results have been presented at the 9th International Symposium on Ultra Clean Processing of Semiconductor Surfaces (UCPSS) held in Bruges, Belgium, September 22-24, 2008.

UCPSS is a bi-annual conference organized by IMEC since 1992. The symposium covers contamination, cleaning and surface preparation in mainstream large-scale integrated circuit manufacturing. This edition was preceded by

a tutorial session given on September 21st by leading experts.

The success of the meeting can be measured by the large number of participants - 290 - from all over the world. This large attendance, despite difficult business conditions, is an indication for the cleaning challenges to be expected in future technologies.

Continuous scaling and broadening of the field involves new materials and approaches, each leading to new cleaning challenges, with tighter specifications. The UCPSS has become a prime forum for exchange and dissemination of new cleaning technologies. In this perspective we already look forward to its tenth edition to be held in 2010. Information concerning future and past editions of this symposium can be found on www.ucpss.org.



Novel quantitative technique for studying electrical defects in dielectric stacks

IMEC proposes trap spectroscopy by charge injection and sensing (TSCIS) as a novel and powerful method for studying electrical defect bands in dielectric materials. This measurement technique meets the current need to quickly and accurately characterize defects in different dielectric stacks in order to timely optimize and eventually implement them in an integrated circuit.

TSCIS is a quantitative and spectroscopic technique that provides detailed information on the density profile and trap energy level of both shallow and deep electrical defects in dielectric materials. It has an excellent resolution (for trap densities down to 10^{17}cm^{-3}) and is capable of distinguishing between different process variations.

The method consists in applying a voltage V_{ch} (which is larger than the threshold voltage V_{th}) at the gate of an NMOS transistor during increasing time intervals (from $\sim 10\text{ms}$ to 1000s). Consequently, dielectric traps inside the bulk of the dielectric are charged by direct tunneling of electrons from the inversion layer. In between the charging intervals, the gate voltage is switched for about 3ms to a voltage V_{sense} which is lower than V_{th} . The interruptions at V_{sense} are short such that all charge sufficiently far away from the interface remains in the dielectric. To determine the trapped charge density, the change of the source-drain current I_{SD} is measured at V_{sense} . This

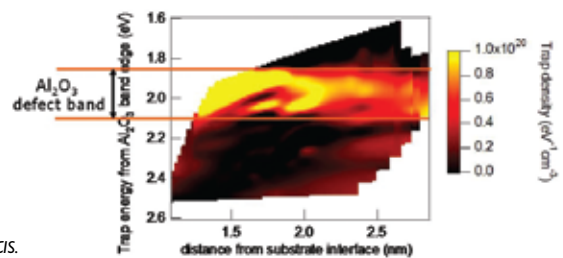
change is converted into a V_{th} shift. After discharging the sample completely, the same procedure is repeated for higher values of V_{ch} . The final result shows the V_{th} shift vs. the charging time for a range of V_{ch} values. These data are fed into an algorithm that allows plotting the defect density vs. trap position and trap energy.

The TSCIS method has been applied to a variety of material stacks, including SiO_2 , $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{Al}_2\text{O}_3$ and $\text{SiO}_2/\text{Al}_2\text{O}_3$. In the latter example, it was found that crystalline Al_2O_3 has a defect band with a trap density that varies depending on the processing details. In optimized Al_2O_3 , this trap density can be reduced to below 10^{19}cm^{-3} and the defects appear in a narrower energy range below the conduction band. IMEC has independently modeled the retention behavior in the written and erased state of a floating gate memory with an Al_2O_3 interpoly dielectric. This required the presence of an Al_2O_3 defect

band with identical energy level and trap density, confirming the consistency of IMEC's results. Interestingly, it was also observed that electric stress-induced traps in Al_2O_3 are deep and therefore different in nature from process-induced defects.

The development of this new methodology is an important contribution to the characterization and integration of dielectric stacks. For example, in a TANOS ($\text{TaN}(\text{TiN})/\text{Al}_2\text{O}_3/\text{Si}_3\text{N}_4/\text{SiO}_2/\text{Si}$) stack, the defect density and spectrum of Al_2O_3 are important as they influence the reliability characteristics of the stack. TSCIS also allows for fast screening of new dielectric materials. For such developments, quick and accurate defect characterization methods are indispensable.

These results have been presented at the IEEE International Electron Device Meeting (IEDM) 2008.



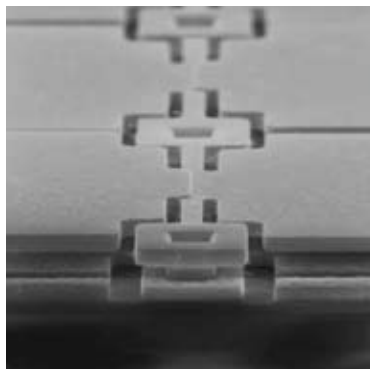
Defect band in crystalline Al_2O_3 measured by TSCIS.

News from IMEC's CMORE platform

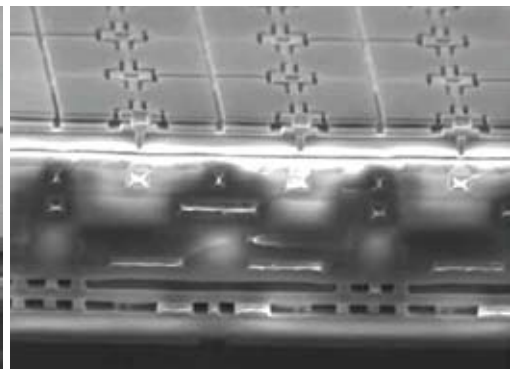
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IMEC builds reliable 11 megapixel micro-mirror array for high-end industrial applications

IMEC's CMORE initiative offers cost-effective solutions for monolithic co-integration of heterogeneous technologies. The services offered range from development-on-demand, over prototyping, to low-volume production. These services profit from the expertise in many research areas available at IMEC. The CMORE solutions are implemented in IMEC's 200mm fab with advanced packaging capabilities, such as 3D integration. The two process platforms involved are a $0.13\mu\text{m}$ CMOS process and a versatile SiGe above-IC MEMS process. On customer demand, the CMORE solution can be migrated to IMEC's 300mm fab.



Top view of individual mirrors and hinges.



Cross-section of the integrated micro-mirror array, showing the mirrors on top of the 6 layers of interconnect.

IMEC fabricates SiGe-on-insulator substrates with high hole mobility

IMEC has used the Ge condensation technique to produce high crystalline quality and high hole mobility SiGe-on-insulator (SGOI) substrates. For a SGOI with 93% Ge content, hole mobilities up to $400\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ have been obtained. The availability of such substrates is an important step forward for the further development of Ge technology as a candidate for ultimate device scaling.

Thin SGOI substrates with Ge contents ranging from 42% to 93% have been produced using the Ge condensation technique. This method is based on the epitaxial growth of a Si-rich SiGe layer on a silicon-on-insulator (SOI) substrate, followed by a high-temperature selective oxidation of Si atoms to condense the Ge atoms in a thinner, Ge-rich SiGe layer. Different Ge contents can be obtained by stopping the process after the first, second or third stage of a 3-step oxidation process. Intermediate annealing steps in Ar during the condensation process are found to be crucial to get high-quality and uniform SGOI substrates.

The electron mobility of the SGOI layers dramatically decreases for Ge contents above 50% while the hole mobility increases with

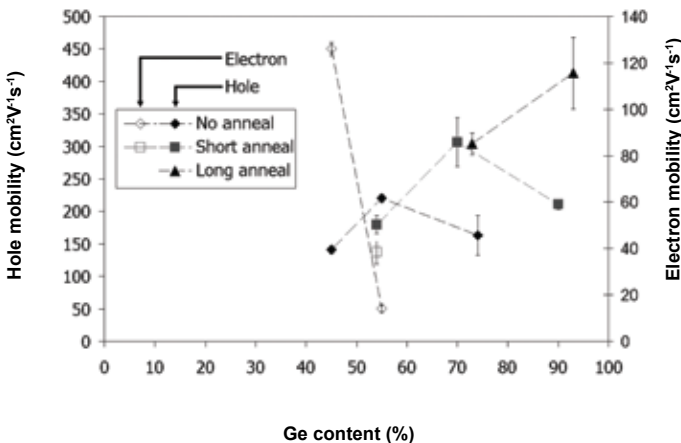
increasing Ge content. These results are obtained from pseudo-MOSFET measurements. They also reveal an increasing hole mobility along with an improved uniformity and crystalline quality of the films. Excellent hole mobility of approximately $400\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ is measured on a 27nm SGOI with 93% Ge. This is a factor 3 improvement over state-of-the-art SOI wafers with a similar thickness, and a factor 2 improvement over strained SOI substrates.

Nevertheless, the properties of the buried oxide (BOX) (fixed charge, interface traps) are observed to degrade with increasing Ge content. Therefore, a further development will consist in optimizing the quality of the interface to avoid jeopardizing, via interface coupling, the electrical performance

of devices processed on the top surface of such SGOI substrates.

These results demonstrate that Ge condensation is a suitable technique for producing Ge-on-insulator (GeOI) wafers with excellent structural and electrical properties. In addition, the technique enables wafer scalability and allows the production of ultra-thin, and, hence, cheap GeOI. Such substrates contribute to a further development of the Ge technology that might be used in future MOSFET applications. GeOI substrates additionally offer a good electrostatic control for short channel effects and reduced junction capacitances.

These results have been presented at the 2008 Electrochemical Society Conference (ECS).



Hole and electron low field mobility of SGOI substrates as a function of the Ge content and as a function of the type of anneal used in addition to the condensation.

Courses

IMEC's training center MTC organizes

Introduction course to Cadence-based full custom design

January 26-28, 2009, IMEC, Leuven, Belgium

The course targets designers new to full custom (or transistor-level) design, layout, verification and characterization, and/or new to Cadence DFII software. The participants will explore a design flow of simple analog circuits through hands-on Cadence sessions.



More information and a full overview of courses on www.imec.be, Education.

IMEC demonstrates fully solution-processed organic solar cells

IMEC has developed a novel method that allows fabricating good-quality solution-processed electrical contacts to organic devices. The method uses an advanced spray coating technique that earlier allowed fabrication of the active layer of an organic solar cell (OSC). Hence, fully solution-processed OSCs with power conversion efficiencies exceeding 3% could be demonstrated. The method is scalable to roll-to-roll production and allows fast and cheap large-area processing of OSCs on rigid and flexible substrates.

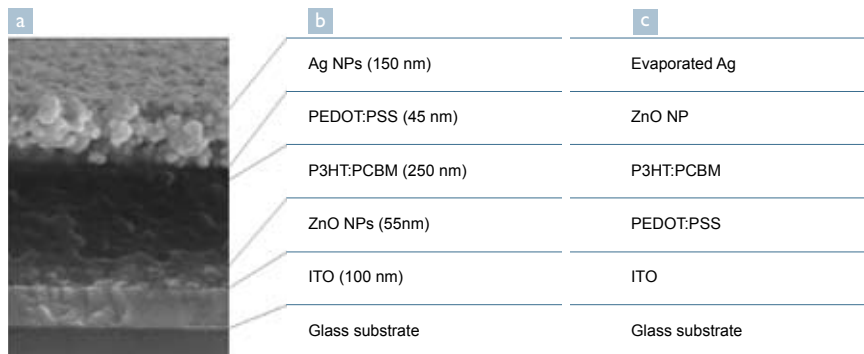
An innovative method based on solution processing has allowed the formation on an organic semiconductor layer of electrical contacts with good electrical conductivity (in the range between 10^4 and 10^6Scm^{-1}) and good stability. The metal contacts are formed by spray coating a Ag nanoparticle ink using a commercially available airbrush powered by a N_2 gas. A sintering process at a temperature between 100°C and 180°C is then applied during which the nanoparticles melt to form a continuous, highly conductive layer. In an earlier announcement, the potential of the spray coating technique was already demonstrated for processing the active layer of an OSC. Advantages of the technique over e.g. inkjet printing or gravure printing are the ability to cover relatively large areas, the scalability to roll-to-roll production methods and its compatibility with the underlying layers.

For the production of fully solution-processed OSCs, an inverted organic photovoltaic cell structure is further proposed. In such a structure, the cathode or electron extracting contact is formed *before* providing the organic semiconductor layer, and the anode or hole extracting contact is formed *after* providing the organic semiconductor layer. If the cathode would be formed after providing the organic semiconductor layer, an electron collecting barrier would be required on top of the active layer to avoid damage of the process for forming metal contacts to the underlying layer. Solution processing of such a barrier layer (comprising e.g. ZnO or TiO) would lead to a morphology that would still allow penetration from e.g. Ag nanoparticles through the barrier layer and would decrease the solar cell efficiency. For the anode, a hole collecting barrier (e.g. poly

(3,4-ethylenedioxythiophene) poly(styrenesulfonate) or PEDOT:PSS) with sufficient thickness can be processed on top of the organic layer to prevent possible damage. The Ag comprising anode is then spray coated on top.

By using the above methods, organic photovoltaic cells have been fabricated. All the layers of the poly(3-hexyl thiophene) (P3HT):(6,6)-phenyl C61-butyric acid methyl ester (PCBM) based solar cells were deposited from solutions on indium-tin-oxide (ITO) patterned glass substrates. Devices show power conversion efficiencies of approximately 3%, a performance which is comparable to that of the evaporated reference devices. In particular, they are characterized by high short-circuit current, well above $10 \text{mA}/\text{cm}^2$. The sintering of nanoparticles was performed at temperatures below 150°C , values which are compatible with the production of devices on flexible substrates such as polyethylene naphthalate (PEN) foils.

The procedure outlined here allows the fabrication of fully solution-based organic solar cells via a fast and easily scalable process.



(a) Scanning electron microscopy (SEM) cross-section and (b) structure of a fully solution-based organic photovoltaic cell with inverted structure; (c) for comparison, how a classical structure with evaporated materials would look like.

News from IDESA

MTC is prime contractor for IDESA, a project in the EC 7th Framework Program. IDESA's goal is to support universities to keep up with the evolution of IC design and implementation flows for deep submicron technologies. The project offers the following training courses:

- Advanced digital physical implementation flow
- Advanced analog implementation flow
- Advanced RF implementation flow
- Design for manufacturability – preparing for the 65/45nm design

More information and course calendar on www.idesa-training.org.

IDESA frequently organizes 3-hour tutorials on design issues relating to design for the 65 and 45nm nodes. If you would want to attend these tutorials, please notify training@imec.be.



IMEC develops innovative active ADSL-POTS splitter

CMST (Centre for Microsystems Technology), as part of the association IMEC has with Ghent University, in cooperation with Alcatel-Lucent, has developed an active ADSL-POTS splitter. In the novel splitter, part of the transformers are replaced by active impedance synthesis circuits, resulting in a footprint reduction of 40%, while still retaining full splitter specifications (ETSI TS 101 952-1-1 v1.2.1).

An ADSL-POTS splitter is a low-pass filter implementing two functions. First, it prevents the ADSL signals (32kHz to 2.2MHz) from interfering with the regular telephone service, which uses POTS signals (300Hz to 4kHz). Second, it blocks POTS transients from disturbing the ADSL service. POTS transients contain high-frequency components; examples are the on/off hook and ring start/stop events. An ADSL-POTS splitter functions in two directions: the incoming POTS signals are filtered out so they don't interfere with the ADSL, and the outgoing POTS signals are put back onto the line without disturbing the outgoing ADSL broadcast.

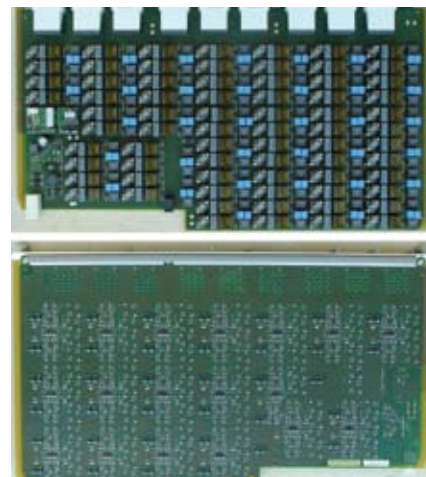
A major drawback of traditional, passive ADSL-POTS splitters is their large footprint due to the bulky transformers that are needed. The transformers are so large because of the relatively low cut-off frequency, and because of the high

transformer saturation levels related to the high DC currents and current spikes during POTS transients. For every ADSL subscriber, there is an ADSL-POTS splitter needed, so there is a large demand for smaller ADSL-POTS splitter solutions.

In this new ADSL-POTS splitter, the footprint is reduced by replacing part of the transformers by an active impedance synthesis circuit. This circuit fully assumes the function of the omitted transformers and is designed to specifically realize an inductor with a controllable inductance as function of frequency. In this way, a passive stage of the ADSL-POTS splitter can be replaced with a smaller active subcircuit, while still implementing full splitter specifications.

This passive-to-active conversion of the ADSL-POTS splitter results in a footprint gain of more

than 40%. The number of ADSL-POTS splitters that fit onto one splitter board (size $\approx 40.5\text{cm} \times 22.58\text{cm}$) increases from 48 to 72.



PCB panel with 72 active POTS-ADSL splitters. The top contains the passive components and a DC-DC converter; the bottom features the active circuits and the voltage protection circuits.

INDUSTRY LINK

Molecular instrumentation spinoff TRINEAN shapes up for production

Recently, IMEC's spinoff Trinean closed a new round of financing, allowing it to start production, to bring its products to the market, and to develop new applications. Trinean was founded in September 2006, together with Ghent University, as an innovative player in the sector of molecular instrumentation.

Trinean's optical instruments are based on two scalable technologies: microfluidic plastic chips to handle microliter droplets, and innovative multichannel spectrometry. Combining these two will improve measurements in a broad range of applications: it will reduce the sample size and increase the throughput and measurement range, resulting in cheaper, faster, and more accurate measurements.

Trinean's technology is first targeted to measure DNA/RNA concentrations in microvolumes. Up to now, the biotech industry had to sacrifice valuable amounts of DNA/RNA because concentrations

could only be determined in larger-than-microliter volumes. Other applications that will be targeted are profiling of drugs (for in vitro ADME testing), measuring protein concentration, mixing and measuring enzymes, and clinical diagnostics.

As a first product, Trinean has developed a polychromatic microliter spectrophotometer with corresponding microfluidic plastic chip with 16 or 96 reservoirs. This product allows full-spectrum, high-throughput UV/VIS spectroscopic measurements in droplets of between 0.5 μL and 2.5 μL . These measurements are both fast and automated, doing a full spectrum analysis of 96

samples in less than 4 minutes. Compared to state-of-the-art instruments, Trinean's platform shows a 6-fold increase of the measurement range, with a 500-fold reduction of the sample size. The spectrometer can be integrated in both manual and automated labs.

For more information, visit www.trinean.com

Microfluidic plastic chip for measuring droplets down to 0.5 μL .



Low EOT SrTiO₃ MIM capacitors on TiN electrode for future DRAM nodes

A low-temperature atomic layer deposition (ALD) SrTiO₃ (STO) process is proposed to produce low-cost, easy-to-manufacture TiN electrode metal-insulator-metal capacitors (MIMcaps) for future dynamic random access memory (DRAM) applications. Low leakage and low equivalent oxide thickness MIMcaps could be demonstrated.

IMEC, in collaboration with ASM, has fabricated MIM capacitors with excellent leakage-EOT behavior by using a low-temperature ALD STO deposition process on an ALD TiN bottom electrode.

The availability of such MIMcaps is indispensable for future DRAM nodes. STO was already considered a promising alternative to the currently used ZrO₂/Al₂O₃/ZrO₂, but, so far, the proposed deposition techniques turned out to be incompatible with high aspect ratio DRAM applications or could not be used in combination with TiN.

The deposition technique proposed in this work consists in depositing STO layers using ALD at reactor temperatures in the 250°C-300°C range. An appropriate ALD precursor system (including Sr(t-Bu₃Cp)₂, H₂O, and Ti(OCH₃)₄) was used and the deposition variables, composition and post-

deposition processing were carefully optimized. By changing the Sr precursor and the Ti precursor pulse sequence, ALD allows the growth of a wide compositional variety of STO films from pure TiO₂ to Sr-rich. STO films in the 7-30nm range were grown on TiN bottom electrodes. In ALD, the STO growth is determined by self-limiting surface reactions, guaranteeing conformal deposition of STO in high aspect ratio structures.

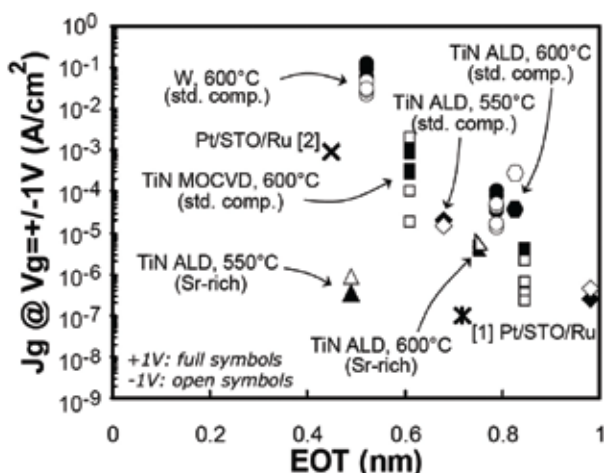
For thin films, the Sr-rich composition gives an overall lower leakage than Ti-rich films and films with a composition close to stoichiometric 1:1.

For a 7.5nm Sr-rich film, an excellent low leakage behavior is observed, with $J_g(+1V)=3.5 \times 10^{-7} \text{ A/cm}^2$ and $J_g(-1V)=8.9 \times 10^{-7} \text{ A/cm}^2$, and extracted EOT values are as low as 0.49nm. These are the lowest leakage values reported so far for STO with ~0.5nm EOT. It was also found that the leakage conduction

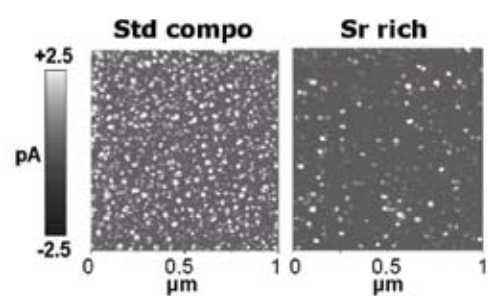
occurs through the bulk of grains and follows the topography (higher topography corresponds to a higher leakage). In a Sr-rich composition, the density of leakage spots is lower than in a 1:1 film, resulting in a better leakage behavior. 550°C turned out to be the optimal annealing temperature, since higher temperatures increase the EOT without leakage reduction and lower temperatures result in non-crystalline films.

EOT extraction for a Ti-rich composition was difficult due to the high conductivity/high leakage observed in these films.

A comparison with recent published data for STO/Ru films shows that this work enables STO/TiN at competitive leakage-EOT performance.



Positive and negative gate leakage (at $\pm 1V$) vs. EOT of standard composition (1:1) and Sr-rich ALD SrTiO₃ films on various bottom electrodes and after different thermal treatments.



Current maps of thin standard (1:1) and Sr-rich STO films on ALD TiN after rapid thermal annealing at 550°C.

These results have been presented at the IEEE International Electron Device Meeting (IEDM) 2008.

World's first UHF rectification using organic diodes

Within the framework of Holst Centre, the world's first plastic diode operating in the ultra-high-frequency (UHF) band has been developed and reported at the IEEE International Electron Devices Meeting 2008 in San Francisco.

For organic-electronic applications such as RFID-tags, the rectifier is one of the most critical components. The rectifier is responsible for converting the electromagnetic energy of the incoming RF signal captured by the antenna into a DC operating RF signal voltage that powers the transponder chip on the tag. Plastic transponder chips that hold the promise to result in low-cost tags have been shown in the past years. However, the antenna itself forms a significant part of the cost of an RFID tag. Antennas for the UHF frequency band (operating at 433MHz, 869MHz, 915MHz)

are smaller and cheaper than antennas for HF (13.56MHz), therefore UHF is the preferred frequency band for ultra-low-cost tags. For the first time, researchers have been able to make an UHF rectifier (operating at 433MHz and 869MHz) with a plastic diode. This is therefore not only a scientific breakthrough, but it also opens the door for low-cost plastic electronic tags.

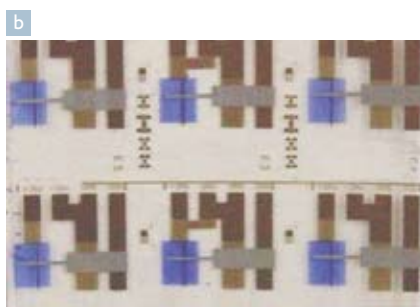
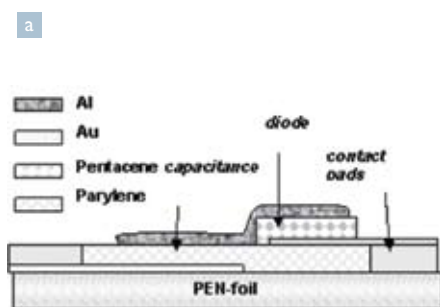
Technical details

The rectifier presented at IEDM was made using a 160nm thin film of purified pentacene sandwiched

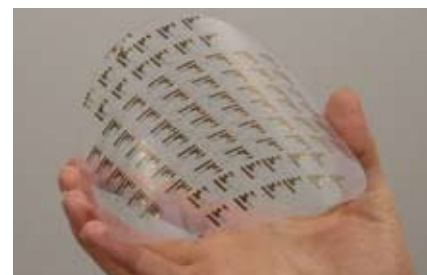
between Al and Au electrodes on glass. The diodes have a reverse breakdown voltage exceeding 25V and a charge carrier mobility of $0.15\text{cm}^2/\text{Vs}$.

The diodes were integrated with capacitors into rectifiers on a plastic foil. These integrated rectifiers operate up to a frequency of 869MHz. The rectified DC voltage at 869MHz is 4.5V. Further increases of the voltage level will be possible using a more complex rectifier.

The work was done within the framework of the Holst Centre research program on organic circuitry, in close collaboration between IMEC and TNO Eindhoven (the Netherlands), and was co-funded by the European project POLYAPPLY.



(a) Schematic and (b) picture of an integrated rectifier on foil (PEN=polyethylenaphthalat).



Integrated plastic rectifiers on foil.

Novel gas sensor characterization facility supports sensor

In the framework of Holst Centre, IMEC has installed an experimental set-up that provides a flexible platform for gas sensor testing. This gas sensor characterization facility will support the ongoing developments of (bio)chemical sensors.

IMEC has developed a gas sensor characterization facility comprised of a gas mixing set-up, a custom-made probe station, and a semiconductor parameter analyzer. This experimental set-up was built to complement the development of gas sensors by providing a flexible platform for testing.

The samples are contacted by means of adjustable probes in an enclosed, controlled environment. As a result, the devices can be monitored in the middle of the fabrication process with no need to bond them in a package. Electrical measurements can be performed while gases are flowing with varying

concentrations. Therefore, transient responses and responses to increasing concentrations can be measured without opening the vessel. Several different gases can be used in the set-up because gas mixing components can be added or changed easily.

A detailed description of the different elements of this gas sensor characterization facility is given below:

Gas mixing set-up

A stream of gas with a well-defined composition is generated with a gas mixing set-up. Nitrogen or

dry air can be chosen as the main gas stream with an optional water bubbler for humidity control. A variable concentration of a gaseous analyte or a vapor can be obtained by injection of a trace into the main gas flow. Concentrations can be adjusted to application-relevant levels.

Probe station

The stream of gas from the gas mixing set-up is led through to a custom-made four-probe station. This includes a small chamber where the sample is located and contacted by four electrical probes that are vacuum sealed. A controlled atmosphere is thus created within the confined space of the chamber, which can contain a 150mm diameter wafer. Gas is continuously flowing through the chamber to avoid concentration changes. The chuck temperature can be controlled in a range from -200°C to $+200^{\circ}\text{C}$. The complete probe station was manufactured by

IMEC demonstrates processor for energy-efficient computation of biomedical signals

In the framework of Holst Centre, IMEC has successfully demonstrated its processor for energy-efficient computation of biomedical signals. This functional demonstrator proves the importance of on-node processing to reduce radio communication.

The need for continuous radio communication can be a significant energy bottleneck for a sensor node system, prohibiting its autonomous operation. Holst Centre, in collaboration with Philips Research Eindhoven, aims to reduce this bottleneck by optimizing on-node processing of biomedical signals. The goal is to reduce the energy consumption, to achieve a long operational lifetime on small batteries and ultimately, for some applications, to run the sensors on scavenged energy only.

The biomedical processor was successfully demonstrated to reviewers of the EU project Wirelessly Accessible Sensor Populations (WASP). The WASP project aims to build electronic aids to assist us in our daily lives and to improve our quality of life using wireless sensor nodes. The project especially addresses health care monitoring, elderly care monitoring, and herd control monitoring.

For the demonstration, an electro-cardiogram (ECG) algorithm was used that detects R-peaks of a QRS waveform. The ECG signals were sampled with

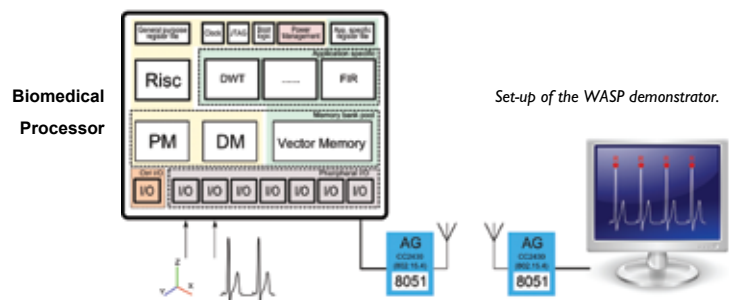
IMEC's proprietary ultra-low-power biopotential ASIC and then processed with the biomedical processor. Additionally, also 3D accelerometer signals were sampled. The radio transmission, containing either unprocessed or processed data, was sent to a PC via the AquisGrain nodes of Philips Research. When the operation was switched from raw, unprocessed data transmission to summarized, processed data, the radio communication was significantly reduced.

The biomedical processor consists of a general, RISC-like issue slot for controller operations. It

can be extended with dedicated issue slots for energy efficient kernel computations. Adding vector instructions that operate on multiple data streams will provide even further optimization.

IMEC keeps improving this biomedical processor for energy-efficient computations of biomedical signal processing in the frame of its HUMAN++ program. Further research is ongoing in such fields as low-power memory, standard cell circuit design, power management, system level interconnections, and ASIP design for e.g. ECG and EEG.

For more information on WASP, visit <http://www.wasp-project.org/>



development

Materials Development Corporation. A magnifying stereoscope is mounted on the set-up to facilitate the placement of the probe tips on the contact pads.

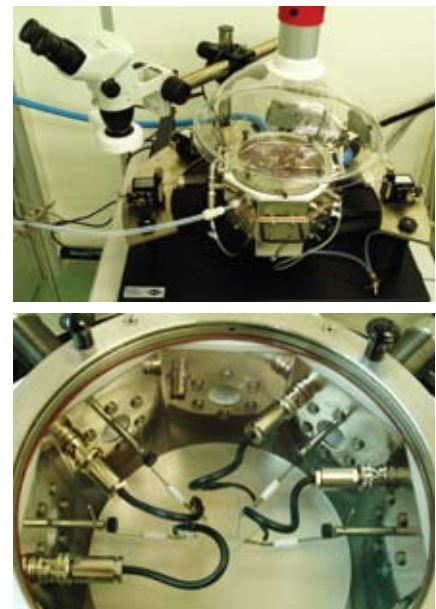
Semiconductor parameter analyzer

The sensor response to the gaseous analyte is monitored by a semiconductor parameter analyzer (Agilent B1500). Four source-meter units are available so that more complex devices can be characterized. The maximum voltage and current ranges are 100V and 100mA, respectively. The minimum voltage and current resolutions are 0.5 μ V and 1fA, respectively. A complex-impedance measurement unit (from 1kHz to 5MHz) is also included in the system. Resistive, capacitive, and inductive measurement geometries are thus also possible.

Computer-controlled hardware makes it possible to fully automate the measurement sequences.

The gas sensor characterization facility was built in the frame of the activities on sensors and actuators, which focus on the development of generic sensor technologies for low-power, wireless and autonomous electronic devices. The current interest is focused on (bio)chemical sensors. Applications are found in the industrial, domestic, environmental, agricultural, logistical, and medical fields.

The novel gas sensor characterization facility at Holst Centre.



First demonstration of flux quantization in a superconducting IMEC circuit as a potential candidate for a solid-state quantum bit

IMEC, in collaboration with the Universities of Louvain-La-Neuve (UCL) and Bologna, has demonstrated for the first time ever a controlled quantum effect in a Si-based superconducting circuit. This achievement clears a major obstacle towards the realization of a true logic device that can switch between two quantum states, and, hence, towards real quantum computing.

In view of the great potential of quantum computing, IMEC proposed a circuit as a quantum bit candidate. The circuit consists of three superconducting rings, inter-connected by two ferromagnetic cores to form a superconducting transformer. Simple (DC) I/V measurements are performed at the outer rings, connected to bonding pads, acting as input/output ports. The I/V signals induce a magnetic field inside the device, enhanced and distributed between the rings by the cores and allow to monitor the central ring. In this way the central ring was accessed for signal input and readout and operated as a logic switch. The team managed to trap one flux quantum inside the circuit, switching the ring between a zero flux ground state and a higher state.

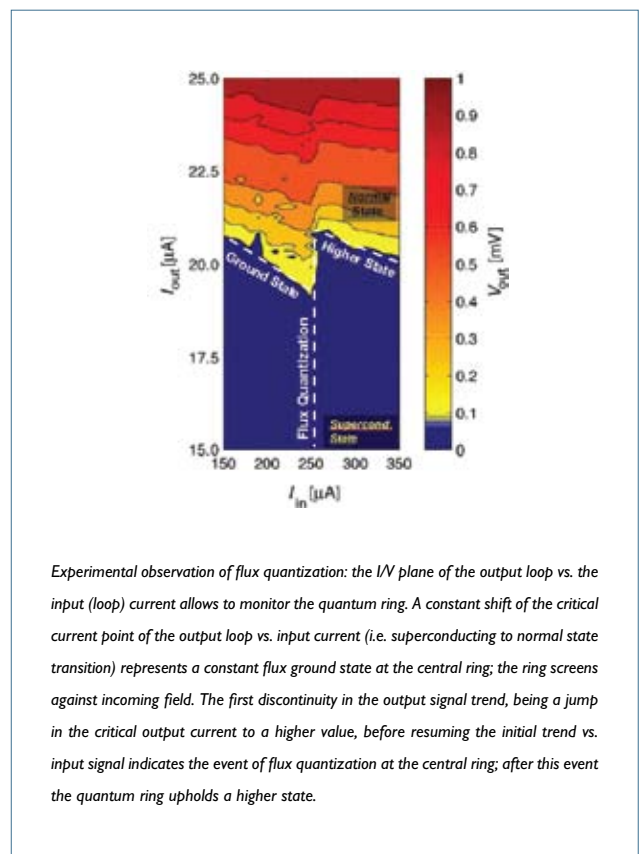
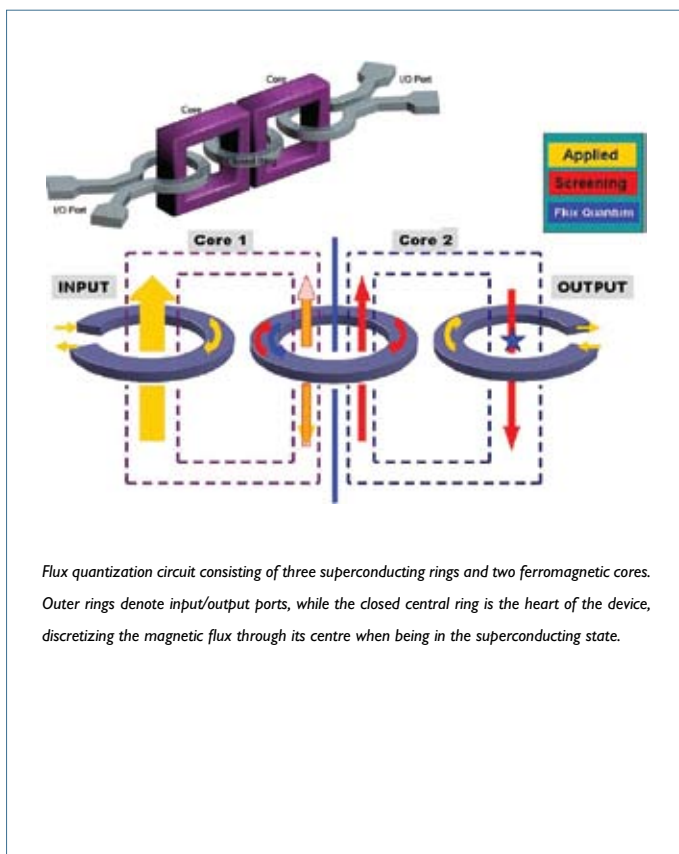
The samples were prepared on 2-inch Si wafers using aluminum (Al) for the rings and nickel-iron

(NiFe) for the cores. Insulating layers consisted of silicon-nitride. A five-layer process flow was used to transfer the design onto the wafers in subsequent litho-metallization-lift-off cycles. The NiFe cores boost up the mutual inductance in the system and allow to guide and enhance the magnetic field transfer between the rings. The Al becomes superconducting at low temperature and the property of flux quantization in a closed superconducting ring is used to drive a DC transformer mode and control/read out the discrete flux state of the central ring. The employed components were in the μm range (planar direction), with rings of about $26.8\mu\text{m}$ diameter and a thickness of 30nm. The layout is flexible in terms of number of rings/cores and employed ring sizes, depending fully on the process specs; physical operation is not compromised.

Low temperature ($\sim 1.2\text{K}$) transport measurements were conducted using cryostat equipment. A modulated (DC) input current signal in the $250\mu\text{A}$ range was sufficient to operate the DC transformer and to induce flux quantization. Monitoring the output loop's I/V plane allowed to pick up the quantization event at the central ring, translating it into a characteristic electrical signature. Furthermore, different physical situations can be distinguished (constant flux state, switch to higher flux state) in the output signal.

These results represent a first milestone for achieving quantum information processing with this concept in future where superposition and entanglement phenomena inside a multi-ring register are required.

These results have been published in Supercond. Sci. Technol. 22 (2009) 025001.



EUROPRACTICE celebrates 2000 multi-project wafer runs

Under the brand name EUROPRACTICE IC service, IMEC offers an ASICs (application-specific integrated circuit) prototyping service and small-volume production. Called multi-project wafer runs (or shuttle runs), the IC designs of several customers, universities, or private companies are collected on a single mask, and manufactured in small prototype quantities. In August 2008, IMEC made its 2000th multi-project wafer run for this highly successful service.



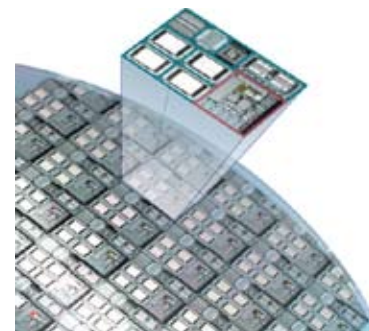
Through the EUROPRACTICE service, universities and companies get easy access to ASIC technology. First of all, IMEC offers help with the design, layout, and tape out of the IC. Next, the multi-project wafer runs allow sharing the expensive mask costs between the designs on the wafer. And finally, the EUROPRACTICE service allows small-volume production - up to a few thousand wafers per year.

For the small-volume production IMEC collaborates with foundries and with assembly and test houses to offer a fully supported solution. With EUROPRACTICE IC service, customers don't have to commit to high-volume production, which could

be a major obstacle for start-up companies and companies with small niche markets.

Up till now, IMEC has supported 650 universities and close to 400 companies from 52 countries. Per year, customers submit around 550 designs to the multi-project wafer runs.

In addition, IMEC provides free technical support to European universities and research institutes. This support is funded by the EC as part of the FP7 project EUROPRACTICE IC4, a project that runs through 2010.



Awards

Gilbert Declerck, CEO, IMEC, has received the **IEEE Frederik Philips Award** as part of the 2008 IEEE Awards Presentations. This award recognizes outstanding accomplishments in the management of research and development, resulting in effective innovation in the electrical and electronics industry in the IEEE fields of interest. The IEEE Frederik Philips Award recognizes Gilbert Declerck for leadership in the creation of international R&D alliances in semiconductor technologies. It is one of the highest professional acclaims that one can receive from one's IEEE peers.

- IMEC's Microelectronics Training Center (**MTC**) was honored with the Semicon Europe **IC Industry Award 2008** in the category education initiative of the year.
- **Anabela Veloso** received the **Best Paper Award** at the IEEE SOI Conference for her paper entitled 'Capping-metal gate integration technology for multiple-VT CMOS in MuGFETs'. (Coauthors: L. Witters, M. Demand, I. Ferain, N. J. Son, B. Kaczer, Ph. J. Roussel, C. Adelman, S. Brus, O. Richard, H. Bender, T. Conard, R. Vos, R. Rooyackers, S. Van Elshocht, N. Collaert, K. De Meyer, S. Biesemans, and M. Jurczak)
- **Joris Van Campenhout** (INTEC, Ghent University, currently at IBM Watson research lab, USA) was awarded the **Alcatel-Lucent Bell prize** for his PhD thesis entitled 'Thin-film microlasers for the integration of electronic and photonic integrated circuits'. (Supervisor: R. Baets)
- **Gunther Roelkens** (INTEC, Ghent University) was awarded the '**Andre De Leenheer-prize**' for his PhD thesis entitled 'Heterogeneous III-V/silicon photonics: bonding technology and integrated devices'. (Supervisor: R. Baets)
- **Karolien Vasseur** has received the **Best Poster Award** at the International Meeting on Molecular Electronics (ElecMol) 2008 for her poster entitled: 'Growth of a perylene derivative and its use in nanostructured bulk heterojunction organic solar cells'. (Coauthors: D. Cheyns, C. Rolin, S. Vandezande (K.U.Leuven), K. Temst (K.U.Leuven), J. Genoe, L. Froyen (K.U.Leuven) and P. Heremans)
- **IMEC** received the '**Top Employers Belgium 2009**' label. This label is granted to companies that exhibit an outstanding HR policy in terms of conditions of employment, promotional opportunities, work atmosphere and work conditions, and education and training.
- **Jay Mody** received the 2008 **IEEE Electron Devices Society PhD Student Fellowship**. The PhD Fellowship Program was established to promote, recognize and support PhD level study and research within the Electron Devices Society's field of interest. Fellowships are awarded for the student's significant ability to perform independent research in the fields of electron devices and for a proven history of academic excellence.
- **Robin Stevens** (ETRO, Vrije Universiteit Brussel) received the **Baudouin Elleboudt Award 2008** for his thesis entitled 'Spatially and directionally adapting transforms for image coding.' (Supervisor: A. Munteanu).
- **Diedrik Vermeulen** (INTEC, Ghent University) received the **Alcatel-Lucent Bell MSc Thesis Award** for his thesis 'Design and fabrication of an integrated transmitter for fiber-to-the-home (FTTH) optical networks'. (Supervisor R. Baets)

Events

2009 International Solid-State Circuits Conference

February 8-12, 2009, San Francisco, CA, USA

The International Solid-State Circuits Conference (ISSCC) is the foremost forum for presentation of advances in solid-state circuits and systems-on-a-chip. This year, IMEC will actively contribute to the conference with 7 papers:

- A Multirate 3.4-to-6.8mW 85-to-66dB DR GSM/Bluetooth/UMTS Cascade DT $\Delta\Sigma$ M in 90nm Digital CMOS.
- A 128b Organic RFID Transponder Chip, including Manchester Encoding and ALOHA Anti-Collision Protocol, Operating with a Data Rate of 1529b/s.
- Integrated Capacitive Power-Management Circuit for Thermal Harvesters with Output Power 10 to 1000 μ W.
- 50-to-67GHz ESD-Protected Power Amplifiers in Digital 45nm LP CMOS.
- A 2mm² 0.1-to-5GHz SDR Receiver in 45nm Digital CMOS.
- A Digitally Controlled Compact 57-to-66GHz Front-End in 45nm Digital CMOS.
- A 57-to-66GHz Quadrature PLL in 45nm Digital CMOS.

More information: www.isscc.org

PESM 2009 – 2nd International workshop on Plasma Etch and Strip in Microelectronics

February 26-27, 2009, Novotel, Leuven, Belgium

Continuing downscaling of semiconductor devices brings new challenges for plasma etch and strip. New materials (high-k and low-k dielectrics, metal gates, phase-shift memories etc.) and new architectures (3D devices, channel-engineered devices etc.) require new etch and strip approaches. IMEC organizes this workshop to bring together people from research institutions and industry to discuss new challenges in plasma etch and strip.

More information: www.pesm2009.be

Smart Systems Integration 2009

March 10-11, 2009, Crowne Plaza Hotel, Brussels, Belgium

Smart Systems Integration is the international communication platform for research institutes and manufacturers to exchange know-how on smart systems integration and to create the basis for successful research co-operations with focus on Europe. Focus of the Conference and Exhibition is on integration issues of miniaturized systems, MEMS, MOEMS, ICs and electronic components. Conference Chair is Thomas Gessner, Fraunhofer ENAS, Germany. Chris Van Hoof, IMEC, is local co-chair. Bert Gyselinckx, IMEC at Holst Centre, will give a keynote presentation on 'Wearable healthcare applications of wireless sensor systems'.

More information: www.mesago.de/en/SSI/main.htm

Embedded Systems Conference Silicon Valley 2009 – Booth #1535

Conference March 29 - April 3, Exhibition March 31 – April 2, 2009

McEnery Convention Center, San Jose, CA, USA

The Embedded Systems Conference Silicon Valley is the ideal forum to learn relevant new skills and to find the latest embedded systems technologies and products. Keep up to date with IMEC's latest developments in this field and visit us at booth #1535 of DSP Valley, the Belgian technology network organization focusing on embedded signal processing system design. More information: www.cmp-egevents.com

DATE09 – Design, Automation and Test in Europe – Rhodes Hall, Level 2, Booth #C21

April 20-24, 2009, Nice Acropolis, Nice, France

The DATE Conference and Exhibition 2009, a leading global electronics event, will this year cover two key themes. The first is a multi-core theme which covers advances and applications including design methods, architectures and programming. The second theme covers systems-on-chip and development of strategies for application-oriented design flows and methods. Visit IMEC at the DSP Valley booth #C21.

More information: www.date-conference.com

2009 European Reconfigurable Radio Technologies Workshop and Product Exposition

April 22-24, 2009, Madrid, Spain

The SDR Forum organizes this workshop to bring together wireless telecommunications equipment manufacturers with their customers and suppliers to explore the evolution of reconfigurable radio over the next several years. Discover IMEC's latest SDR solution, comprising a flexible RF transceiver and programmable baseband platform, for next-generation flexible mobile terminals. IMEC will also present a first step in the evolution from an SDR solution towards a cognitive radio.

More information: www.sdrforum.org

Patents

China

- *Method to make markers for double gate SOI processing, and semiconductor wafers.* (CN 1670908)

Europe

- *Widely wavelength tunable integrated semiconductor device and method for widely wavelength tuning semiconductor devices.* (EP 1 058 358)
- *Method and apparatus for localized liquid treatment of the surface of a substrate.* (EP 1 168 419)
- *Method for fabricating a thin film build-up structure on a sequentially laminated printed circuit board base - MCM-SL/D technology.* (EP 1 226 743)
- *Method and system for producing an improved layer with atomic layer deposition.* (EP 1 728 894)
- *Method for extracting the distribution of charge stored in a semiconductor device.* (EP 1 732 080)
- *Dual tip atomic force microscopy probe and method for producing such a probe.* (EP 1 748 447)
- *Method to control the 'first-to-melt' region in a PCM cell and devices obtained thereof.* (EP 1 886 318)

Japan

- *Method and apparatus for local surface analysis.* (JP 4163938)
- *Method and device for estimating and compensation IQ imbalance.* (JP 4195000)
- *Method for preparing an electroplating bath and related copper plating process.* (JP 4202016)

USA

- *A method to create super secondary grain growth in narrow trenches.* (US 7,452,812)
- *Method of quantification of hydrophylic properties of porous materials.* (US 7,415,902)
- *Composition and method for treating a semiconductor substrate.* (US 7,432,233)
- *Method for designing a micro electromechanical device with reduced self-actuation.* (US 7,439,117)
- *Method for producing a semiconductor device and resulting device.* (US 7,442,635)
- *Method and system for transmitting digital signals between nodes of a network for optimized processing at the receiving node.* (US 7,450,645)
- *Method for optically coupling optoelectronic components.* (US 7,445,390)
- *Method of preparing derivatives of polyarylene vinylene and method of preparing an electronic device including same.* (US 7,446,164)
- *Apparatus and methods for simultaneous surface acoustic wave and surface plasmon resonance measurements.* (US 7,440,085)
- *Power-aware configurable bus driver circuits for lines terminated by a load.* (US 7,449,920)

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ARRM is now IMEC Technology Forum 2009

June 3-4, 2009, Hotel Crowne Plaza, Brussels, Belgium

Celebration
edition

The IMEC Technology Forum is the successor of IMEC's Annual Research Review Meeting (ARRM), which, through the years, has evolved into a true industry networking event. It will take place on June 3 and 4, 2009 and is organized in the frame of IMEC's 25th anniversary. On the first day, prominent speakers from the semiconductor industry worldwide will focus on the future strategy for scaling and non-scaling activities, on the changes in business approach and collaboration opportunities with R&D centers. Additionally, you can attend panel discussions on biomedical electronics and photovoltaics. On the second day, you will be part of the IMEC Research Business Forum. Don't miss this Technology Forum where open innovation is considered of paramount importance.

More information soon in the events calendar on www.imec.be



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