



## Novel drying concepts for single-wafer wet cleaning

*IMEC recently developed two novel fast-drying methods for single-wafer wet cleaning.*

Current IC manufacturing faces major challenges. The transition to 300-mm wafer size has to be accomplished while the overall manufacturing cost continuously needs to be reduced. This leads to different manufacturing concepts and clean room layout. Farm layout

clean rooms, consisting of dedicated bays, will be replaced by flow layouts in which different consecutively performed process steps are clustered, resulting in a major reduction of the wafer transport distance. Single-wafer processing becomes grad-

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## IMEC announces 157-nm lithography process development program



While the 193-nm program is running very successfully at IMEC on the ASML PAS5500/900 step and scan system, IMEC is announcing a new lithography program to start middle of 2001, focusing on the next optical wavelength: 157 nm.

*ASML PAS5500/900 scanner and TELACT 8 for 193-nm lithography*

The main goal of this program is to accelerate the 157-nm resist process developments, which are regarded as a major potential showstopper for 157-nm lithography today. IMEC is currently building up the necessary infra-

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## On-line reconfigurable camera designed with OCAPI-xl

*IMEC has developed a stand-alone network camera that allows capturing and transmitting live images on the Internet. To achieve maximum flexibility and throughput, and to keep power consumption low, the entire application was designed in FPGA technology. Additionally, a design environment called OCAPI-xl was set up to cope with this kind of applications.*

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ually dominant in IC manufacturing. Some critical processing steps such as pre-gate-stack formation and CMP put stringent time constraints on the preceding or subsequent cleaning step. Consequently, the introduction of a single wafer clustered clean is the most straightforward approach for such applications. In general, clustered cleans result in a reduction of the standard deviation of the process control parameters and a reduced cycle time. The inspection loop can be consid-

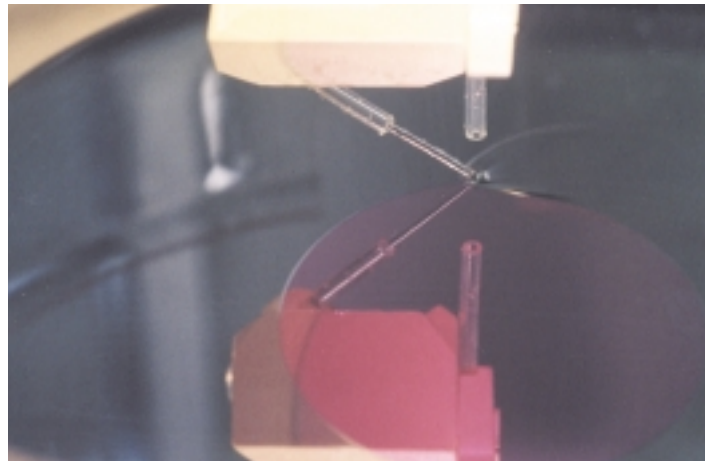
ni™ concept involves a track setup and is developed in collaboration with Steag as part of the Damasclean platform. In the second concept, called Rotagoni™, the wafer remains at its position during the drying process. This method is developed together with Verteq in the Goldfinger platform.

In the Lineagoni™ technique the wafer is slowly pushed through a relatively narrow box-shaped reactor via a narrow entrance and exits

forces and rotational forces. Initially, a continuous flow of rinsing liquid is supplied on the wafer surface through a narrow dispensation tube. The wafer rotates at moderate speed. The dispensation tube slowly moves from the center of the substrate towards the edge. A second nozzle is mounted on the trailing side of the liquid dispense tube. This nozzle dispenses a tensioactive vapour, which reduces the surface tension of the liquid and creates an efficient Marangoni



*Lineagoni™ drying method*



*Rotagoni™ drying method*

erably shortened which can result in scrap reduction. Moreover, cleaning in single-wafer mode opens new possibilities such as single-side cleans.

Clustered cleans have often been associated with dry cleaning. Currently, wet cleaning is largely outperforming dry cleaning. However, one of the major roadblocks for single-wafer wet cleaning is the lack of a fast and high-performance (i.e. water mark-free) drying technique. Therefore, IMEC developed two new drying methods. The Lineago-

the slit at a controlled velocity. The reactor contains the process fluid. The ambient above the liquid is kept at a lower pressure with respect to the pressure adjacent to the chamber close to the slits. The leaking of the liquid can be prevented by tight tolerances on the slit dimensions. At the exit slit, an ambient is present containing a tensioactive vapour. This results in an effective drying of the outcoming wafer.

The Rotagoni™ method is based on interaction between Marangoni

force. The unique interaction between the Marangoni effect and the rotational forces results in a high-performance liquid removal.

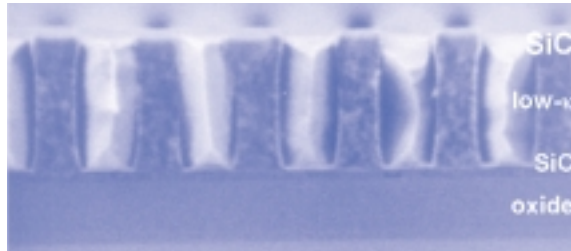
Both techniques show excellent robustness on particle neutrality and high particle removal efficiency. Also excellent cleaning results have been obtained on post Cu-CMP cleaning.

## Characterization and implementation of low-k materials, a real challenge

IMEC devoted a lot of research to the implementation and characterization of low-k materials towards 130 and 100-nm technology nodes. The investigations provide a good selection for low-k materials.

Integration of multilevel metallization in deep-submicron technologies require major changes in material and technological concepts to decrease wiring delays and interline capacitance. It is clear that Cu is needed as alternative for Al in these advanced deep-submicron processes. Low-k dielectrics are required as insulator for critical products, such as high-density and high-speed applications. Low-k materials are still subject to a lot of material characterization. IMEC has devoted a lot of research to the characterization and implementation of both spin-on and CVD dielectrics.

The lowering of the k-value is achieved by the increase of free volume in the matrix material or by adding porosity. Therefore, measurement of the free volume and the characterization of pore distribution, both in size and in shape (open or closed pores), are essential. To do this, IMEC has developed a wafer-level porosimetry tool based on spectroscopic ellipsometry. The technique allows a direct



Cross-section SEM image of a meander/fork structure showing 0.2- $\mu\text{m}$  Cu trenches. The "fake" bowing is induced during SEM imaging.

study of the effect of process steps on the dielectric film properties, most importantly the effect of plasma and chemical treatments. This wafer-level porosimetry has been used to characterize in detail density, free volume and interconnectivity of both porous and non-porous materials after deposition and after process steps such as plasma treatment, chemical treatment etc. The relation between the material properties using real processing conditions and the electrical performance at critical dimensions provides valuable information in the debate of the low-k dielectric of choice.

For the research on stress evolution, the dielectric stacks are built up to several layers with various hard masks. SiC is a very promising

hard mask material for its good adhesion properties as well as its diffusion barrier properties. The low-k dielectrics are implemented in single-damascene and dual-damascene modules for full electrical characterization. Interline capacitances have been measured for all categories of materials. The obtained k-values within the narrow spacings are related to the structure and/or composition of the low-k material, the dry etch and post dry etch clean processes and the Cu metallization. In addition, the structures are evaluated for leakage current breakdown etc. The investigations provide a good selection for low-k materials for multilevel integration towards the 130 and 100-nm nodes.

## World's first SuperPON demonstrator

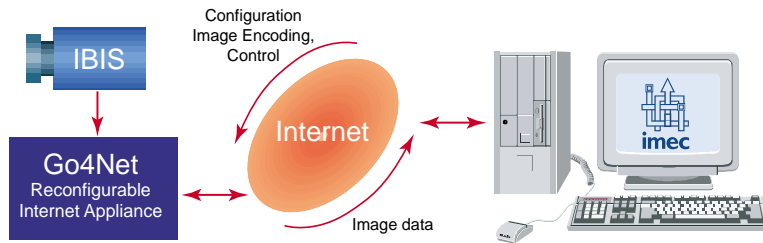
Sustained cooperation between the research department of Alcatel Bell (Antwerp) and the design laboratory INTEC-design from IMEC's associated laboratory INTEC at the Ghent University resulted in world's first SuperPON (an optical-fiber ATM network) demonstrator.

The SuperPON supports up to 2048 network terminations over a range of 100 km, for both broadband and interactive access. The demonstrator realizes a 311 Mbit/s uplink and a 2.5 GHz downlink. This research was made possible by EU funding in the ACTS frame-

work, and by direct funding from Alcatel Bell.

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### Reconfigurable Internet appliance demonstrator

Traditionally, FPGAs are used at places where software implementation does not meet the performance requirements, but still a high flexibility is needed. Configuration data is usually stored near to the FPGA and is read in at boot-up. However, for network applications this reconfiguration data can be stored remotely and delivered through a network connection. This opens a whole new range of applications. For instance, state-of-the-art multimedia algorithms like MPEG-4 can use reconfiguration to implement scalable compression/decompression algorithms that can be transmitted along with multimedia data.

To demonstrate this concept, IMEC has developed a reconfigurable network appliance. Essentially, it consists of an Ethernet (10BaseT) network interface, an FPGA with SRAM, and an application interface. The application interface is connected to an IBIS4-camera, a 1.3 megapixel APS CMOS image sensor developed by IMEC's spin-off FillFactory. The FPGA contains the hardware version of the algorithms needed to format raw image data to a stan-

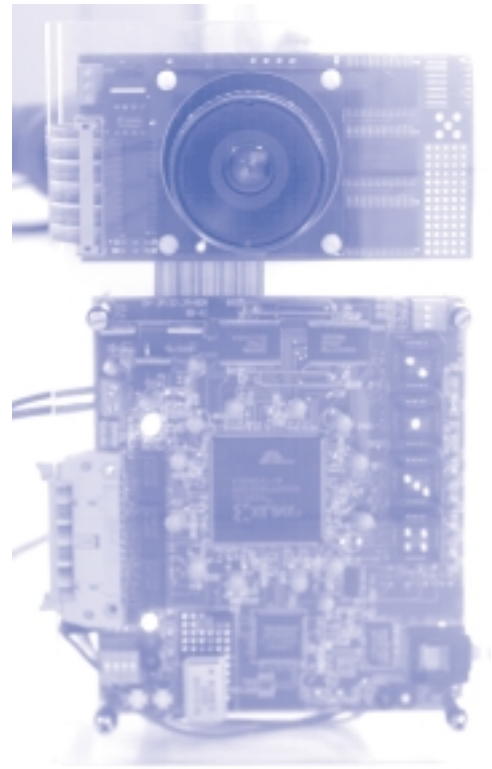
dard format and to transport it over the network to a web browser. This includes support for Internet protocols such as TCP/IP for data transport and HTTP for camera access. Additionally, it also includes an embedded application that captures image data from the camera and converts it into a standard image format (GIF). The appliance including the camera consumes less than 2 Watt, which is a fourfold improvement compared to today's stand-alone embedded Internet camera systems.

To obtain this kind of improvement, dedicated hardware architectures on the FPGA are needed. The complete design was done in OCAPI-xl, a C++ based design environment. OCAPI-xl offers the ability to describe hardware as well as software implementation with a single language (C++) and single system semantics. The semantics adhere to a software design philosophy, and model system behavior as a number of concurrent processes that communicate through primitives like semaphores, messages and shared variables. In addition, OCAPI-xl supports easy integration of existing

software functions through a mechanism called foreign language interface.

Currently, IMEC's research in reconfigurable applications is extrapolating on this demonstrator, to further extend the concept of network reconfiguration. This includes the research in runtime reconfiguration, in which the FPGA configuration is modified at runtime. Technology independent FPGA configuration techniques are being developed, that will allow a single stream of configuration data being mapped on a wide span of FPGAs. Finally, the refinement techniques in OCAPI-xl will be extended to achieve true unified modeling of hardware and software.

### Go4Net looking at itself



continued from p.1

structure for a 157-nm lithography cell. This lithography cell will be focused around a 157-nm mid-field stepper, which will be installed middle of 2001. This mid-field stepper can be situated between small-field microsteppers and full-field scanners. The first have recently started to ship and are focusing exclusively on resist evaluations at 0.6 NA using a reticle magnification of 10 (e.g. International Sematech, Selete). The latter will not be available before 2003. The mid-field stepper has an NA up to

0.75 and uses a reticle magnification of 6, which is coming very close to the NA and reticle magnification of the first generation full-field scanners.

This program is being set up in close collaboration with ASML. IMEC is inviting resist companies and mask shops with an active 157-nm development program that want to have early access to such an exposure tool to test their own developments. Also IC manufacturers are targeted that want to closely follow the 157-nm resist

process and reticle progress and want to generate early experience with 157-nm lithography for initial dry etch and device work.

In 2003, the first ASML 157-nm full-field scanner will be installed at IMEC to which the developed process will be transferred. At that time, a full-field scanner 157-nm development program will be started, very similar to the current 193-nm program but focusing on the 70-nm and 50-nm technology nodes.



70-nm lines printed through focus using the ASML PAS5500/900 ArF step and scan system.

## Technology report

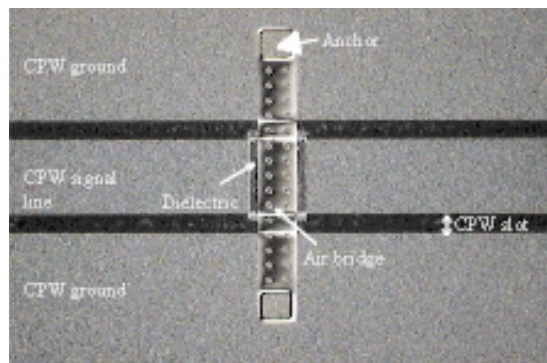
### RF-MEMS devices for wireless communication

First demonstration of RF MEMS (micro-electromechanical) switches and lumped element LC filters has been made. The devices allow building low-loss high-linearity microwave circuits for wireless communication applications.

Wireless communication is showing an explosive growth. Future communication systems require low size and low weight, ever-increasing frequency and high functionality, which necessitate the use of highly integrated RF front-ends. Today, the expensive off-chip passive RF components play a limiting role. On-chip passive components however do not reach the high quality offered by their discrete implementation. A promising alternative is the MEMS technology. IMEC has successfully developed

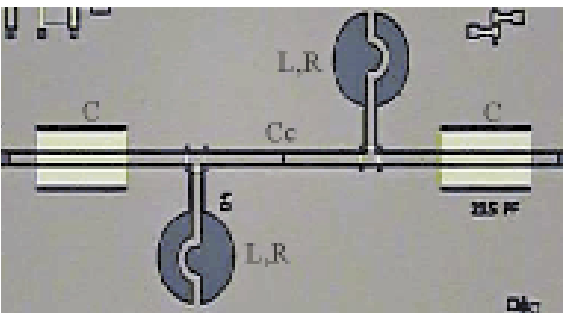
RF MEMS shunt switches and lumped element LC filters. The devices are built on the same sub-

strate using the same process flow. Coplanar waveguides (CPW) are used for the transmission line.



Shunt MEMS capacitive switch implemented on a CPW

The developed shunt switch is implemented on a CPW and behaves as a capacitive switch. The switch consists of a suspended movable metal bridge or membrane, which is mechanically anchored and electrically connected to the ground of the CPW. When the bridge is up, the capacitance of the signal line to ground is low (10 – 100 fF) and



A MEMS second order filter with series capacitive coupling

the switch is in the RF-ON state. Upon activation, the bridge pulls down onto a dielectric layer placed locally on top of the signal line. The capacitance becomes high and the switch is in the RF-OFF state. The area underneath the air bridge is covered with a thin film of tantalum pentoxide with a high dielectric constant. An isolation of 14 dB @ 5 GHz has been demonstrated and values over 30 dB are within the range of the technology. The insertion loss, including both the intrinsic loss of the switch and the loss introduced by the CPW, is approximately 0.15 dB @ 5 GHz. For the lumped-element bandpass LC filters, spiral inductors in combination with air gap capacitors are used. Both half-turn coils and multi-turn coils were realized. Half-turn loops are implemented in the

same metal as used for the CPW. Multi-turn coils use the switch-bridge metal as an air bridge to interconnect the inner part of the inductor to the rest of the circuit. The air gap capacitance can be tuned, and therefore also the center frequency of the filter, by applying a DC voltage across the capacitor plates. The filters were designed to operate at a center frequency between 1 and 10 GHz.

Currently, a single-pole double-throw (SPDT) switch is under development for application in a wireless local area network (WLAN) in the 5-6 GHz band. To establish an integrated system with maximum RF performance, a system-on-a-package (SoP) approach will be used, based on IMEC's MCM-D technology.

## Technology report

### High-level simulation of substrate noise generation by large digital circuits

IMEC has developed a high-level simulation methodology (called Substrate noise Waveform Analysis, SWAN) to accurately and quickly simulate the substrate noise generation of large digital circuits on low-ohmic substrates.

To make future telecommunication devices smaller and cheaper, more and more functions are integrated on one single chip. Also analog functions, such as analog-to-digital converters (ADC), are integrated on these mostly digital ICs. However, substrate noise, generated by large digital circuits, can severely deteriorate the performance of the analog circuits, integrated on the same IC substrate.

To analyze the impact of substrate

noise on the performance of the analog circuits, the amount of noise generated by the large digital part must be known. Due to the large size of the digital circuits, normal circuit simulators such as SPICE can no longer be used to simulate the substrate noise generation. Therefore, IMEC has developed a high-level simulation methodology (SWAN) to estimate the substrate noise in an accurate and time efficient way.

Two major sources of substrate noise generation can be distinguished: noise coupling from the switching gates and noise coupling from the power supply. Which of these two sources will be dominant is determined by the package parasitics. Because the exact package parasitics are not known during the design phase, the SWAN tool can also simulate the substrate noise generation as function of the package parasitics.

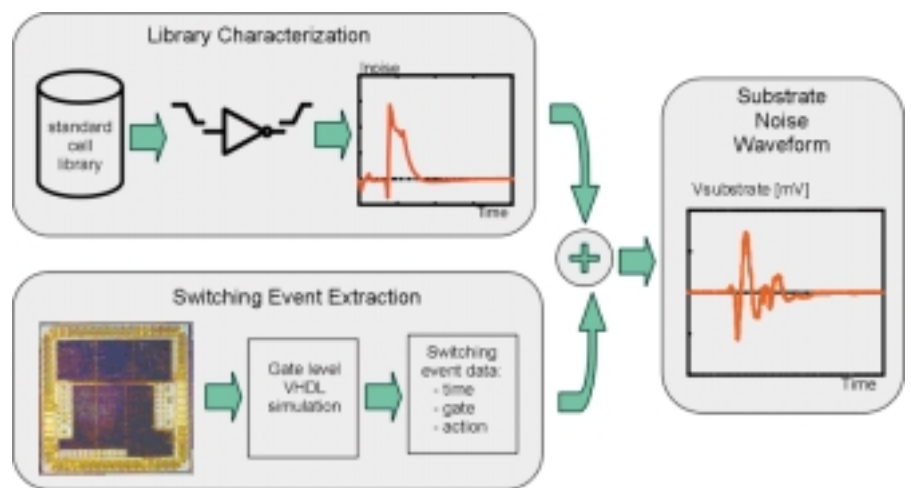
The high-level simulation methodology consists of two parts: standard cell library characterization and substrate noise waveform computation. First, the substrate noise generation and power supply current consumption of all standard cells as function of the switching activity of the cell are extracted and recorded in a database together with a macro-model of the substrate of the cell. This step has only to be done once for a given technology. Next, the substrate noise is calculated for a given design. Therefore, all switching events of each gate are extracted from a standard gate-level VHDL simulation. By combining the noise generation of each gate with the switching activity data, an accurate waveform of the substrate noise signal can be calculated.

The SWAN tool is very helpful for the designer to estimate the noise

impact on the analog circuits and to develop low-substrate noise digital design techniques. Since the tool takes into account package parasitics, an optimal packaging method can be determined. The tool also allows calculating the power consumption of the digital

circuit. The methodology is currently being extended towards high-ohmic substrates.

This research is sponsored by the European Commission and the Flemish IWT (Institute for the Promotion of Innovation by Science and Technology in Flanders).



SWAN methodology flowchart

Technology report

## Poly-SiGe process for post-processing MEMS on CMOS wafers

*The reduction of the deposition temperature of poly-SiGe and the increase of maximum post-processing temperature on CMOS wafers allow post-processing of MEMS on standard CMOS wafers.*

Micro-electromechanical systems (MEMS) such as infrared detectors, accelerometers, gyroscopes, ... are increasingly used. Monolithic integration of MEMS with the driving, controlling and signal processing electronics on the same CMOS substrate can improve performance, yield and reliability as well as lower the manufacturing, packaging and instrumentation costs. The easiest approach for monolithic integration is post-pro-

cessing MEMS on top of the driving electronics, as it enables integrating MEMS without introducing any changes in the standard CMOS fabrication process.

However, post processing limits the maximum fabrication temperature of MEMS in order to avoid any damage or degradation in the performance of the existing electronics. Polycrystalline silicon (poly-Si) has been widely used for MEMS applications, but this mate-

rial requires a high processing temperature (> 800°C) to achieve a low tensile stress and to activate dopants.

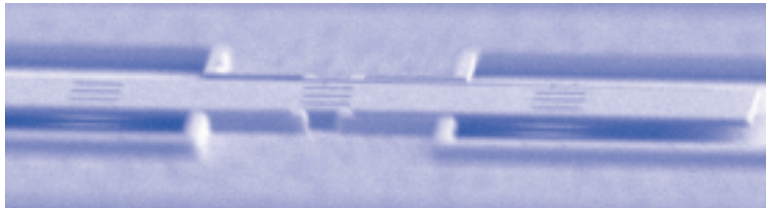
Until now, the maximum post-processing temperature on CMOS wafers with Al interconnections is generally considered to be 450°C. IMEC succeeded to increase the temperature up to 525°C without introducing any significant changes in the standard character-

istics. The front-end is nearly unaffected, whereas for the back-end an increase in interconnection resistance has been observed. This resistance increase can be taken into account during circuit design

and is not considered as a bottleneck.

Polycrystalline silicon germanium (poly-SiGe) is an attractive alternative for poly-Si as it has similar properties, while the presence of

germanium reduces the required deposition and annealing temperature. IMEC could reduce the deposition temperature of poly-SiGe below 510°C, which is compatible with CMOS post processing. The grown layers, with 43 % germanium, have a low tensile stress suitable for post processing MEMS on top of the driving electronics.



First results of surface micromachined poly-SiGe structures deposited at 400°C and annealed at 450°C.

IMEC's research is currently directed towards deposition of poly-SiGe at a temperature of 400°C. This will allow CMOS post-processing without any modifications into the standard characteristics.

### Technology report

## High-level simulation and modeling of mixed-signal front-ends of digital telecom transceivers

The simulator FAST and the modeling tool DISHARMONY make a high-level simulation of a 5 GHz WLAN receiver front-end efficient and accurate.

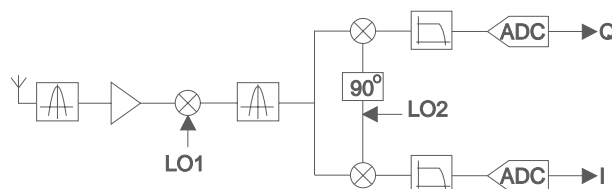
The explosion of the telecommunications market pushes the need for miniaturization and cost-effective realization of transceiver front-ends for digital telecommunications. This requires a study of new front-end architectures. For such studies and for the determination of specifications of front-end blocks, high-level simulation is preferred over rough hand calculations, since a much higher accuracy can be obtained.

The high-level simulator FAST (Front-end Architecture Simulator for digital Telecom applications), being developed at IMEC, can simulate front-ends with detailed models in a reasonable time. The high simulation efficiency is due to several features. First, the signals

are represented in a multi-rate, multi-carrier fashion. This allows an efficient and accurate co-simulation of the RF parts with low-frequency parts. Secondly, the carriers are used locally. For example, RF carriers are neglected in the low-frequency front-end blocks. Prior to simulation, the high-level description of an architecture is

translated into a computational graph that is evaluated during simulation.

The dataflow-type simulation engine of FAST can be coupled with IMEC's OCAPI simulator, in which a detailed description of the digital part of a transceiver can be simulated. In this way, end-to-end simulations of a complete telecom link are possible, allowing an accurate prediction of the bit-error-rate in a reasonable CPU time.

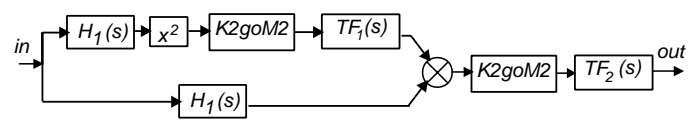
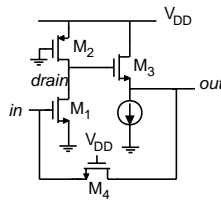


5 GHz WLAN receiver front-end with OFDM input signal having 256 carriers, each with a QAM 16 modulation. Required simulation time: 41.7  $\mu$ s per carrier symbol on a Pentium III 450 MHz processor

For realistic high-level simulations, models are required with an accuracy that goes beyond the rough models that are constructed manually. The program DISHARMONY, developed at IMEC, generates high-level models from a circuit-level description of continuous-time analog front-end blocks such as amplifiers and active filters. The generated models are nonlinear and frequency dependent.

This research is sponsored by the European Commission and the Flemish IWT (Institute for the

Promotion of Innovation by Science and Technology in Flanders).



*High-level model of a low-noise amplifier generated by DISHARMONY. The model consists of static nonlinearities and linear transfer functions that can be readily used in FAST.*

Technology report

## Development of a 0.35- $\mu\text{m}$ SiGe BiCMOS process for RF applications with 80 GHz Fmax bipolar transistors

IMEC is finalizing the development of a selective SiGe HBT (Heterojunction Bipolar Transistor) option for the 0.35- $\mu\text{m}$  BiCMOS generation. Implementation of a selective SiGe base layer improved the performance significantly.

The growing demand for RF applications such as wireless communication, together with the need for higher frequency applications, drive the development of mixed analog/digital CMOS processes with integrated high-performance bipolar transistors. High-performance RF applications require high cutoff frequencies combined with a high Early voltage, high Fmax and low noise.

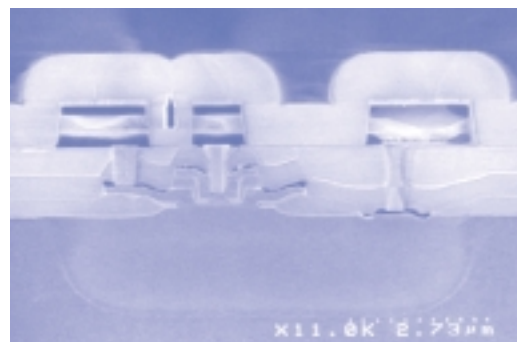
While IMEC's implanted base 0.35  $\mu\text{m}$  BiCMOS process reached already a high RF performance, with Ft of 30 GHz at  $V_{ce}=1\text{V}$ , an Early voltage of 20 V and  $BV_{ceo}=4\text{V}$ , the additional performance improvement by introducing SiGe for the base layer material is significant. To translate high Ft's also in high circuit performance, low device parasitics are extremely important. Therefore, a selective SiGe growth

process was chosen, with a double poly inside spacer self-aligned architecture. The process achieves an Ft of 50 GHz at  $V_{ce}=3\text{V}$  and  $BV_{ceo}=4\text{V}$ . Because of the low device parasitics, a high Fmax of 80 GHz is obtained. Furthermore, the graded Ge profile increases the Early voltage to 100 V. The initially high current gain was traded off against low 1/f noise, by changing the poly emitter process without intentional re-grow of the interfacial oxide.

The selective SiGe base layers were grown in an ASM Epsilon 2000 single wafer reactor at a low process pres-

sure to suppress loading effects. The linearly graded Ge profile has a peak concentration of 15 % and the grown base width is 45 nm. The HBT is integrated in the analog 0.35- $\mu\text{m}$  CMOS process. The process is extended with a full list of supporting devices such as various types of poly resistors, lateral and substrate pnp's, varactors with high tuning range and high Q factors, and a MIM (Metal Insulator Metal) capacitor with 1  $\text{fF}/\mu\text{m}^2$  specific capacitance. The developed SiGe BiCMOS process allows integration of high-performance RF functions.

*Cross section of 0.35- $\mu\text{m}$  SiGe HBT*



## Hybrid phased-array multi-wavelength laser for WDM networks

*A 7-channel multi-wavelength laser for WDM networks was realized using a new hybrid integration technology.*

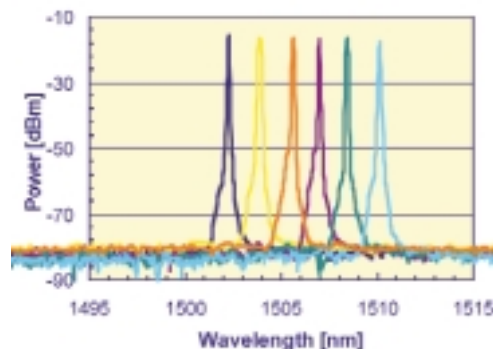
There is a growing tendency in WDM (wavelength division multiplexed) optical telecommunication networks towards the use of smaller channel spacing (down to 50 or even 25 GHz) and larger channel counts (up to 80). This puts very stringent requirements on the

length laser can replace a whole array of discrete lasers or can be used as a wavelength selectable laser.

In the context of the European ACTS-project APEX, IMEC's associated laboratory INTEC (from the Ghent University) has realized such a laser. For that, an optical amplifier array has been integrated together with a phased array multiplexer (fabricated in collaboration with the Delft University of Technology) into one optical cavity. The phased array multiplexer provides for each channel a different wavelength selective amplifier feedback. If the gain of the amplifiers is high enough to compensate for the cavity losses, laser operation is obtained at a frequency determined by the multiplexer.

*Hybridly integrated phased-array multi-wavelength laser module with electrical connections and fiber-chip coupling unit*

To fabricate the device, a hybrid integration technology was developed. The optical amplifier array and the phased array demultiplexer were realized on separate chips and permanently bonded together using an UV-curing epoxy. The module was inserted in a suitable laser package to facilitate an easy optical and electronic access. The realized module consists of seven channels, spaced by 200 GHz (1.6 nm) with a threshold current vary-



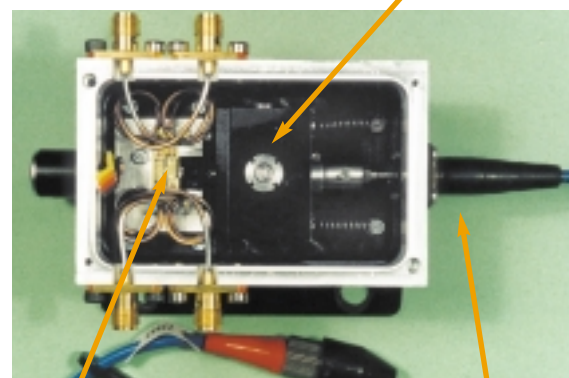
*Superimposed oscillation spectra of a phased-array multi-wavelength laser*

ing between 38 mA and 48 mA. The 3-dB bandwidth is 1600 MHz, which is the highest value ever reported for this type of devices, and is limited by the cavity length. The laser linewidth is very small, namely below 1 MHz.

For more information, contact:  
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*alignment stage with coupling lens*

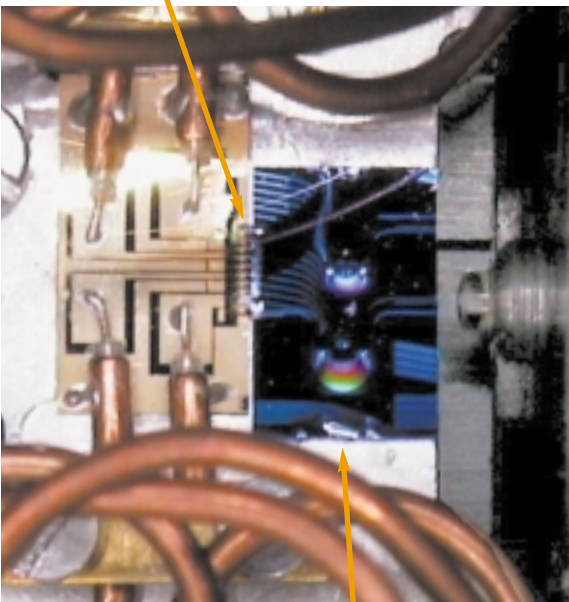
*Photograph of the laser package with the Phased-Array multiwavelength laser*



*PAL-laser*

*optical fibre*

*optical amplifiers on silicon submount*

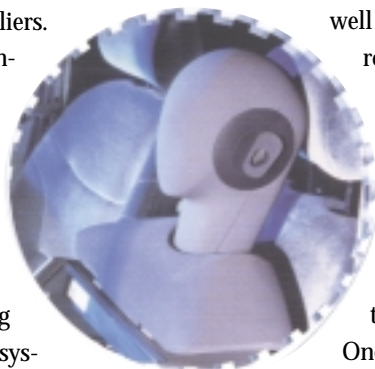


*passive waveguide chip with Phased-Array*

wavelength accuracy and wavelength spacing accuracy of the laser sources. Current systems typically use arrays of discrete wavelength distributed feedback (DFB) laser sources. An alternative is a multi-wavelength source, able to emit several channels simultaneously, each of them separately modulated. Such a multi-wave-

## IMEC puts its know-how in electronics available for Flanders' DRIVE members

In recent years, auto constructors drastically change their relation to their suppliers. More and more constructors chose for global suppliers with their own product engineering department. In addition, due to the growing use of integrated system components, technical requirements are steadily increasing. Therefore, collaboration be-



LMS and Monroe. Other companies have joined the group as well as universities and research institutes. One of them is IMEC. IMEC puts its know-how in electronics accessible for the companies of the consortium. One of the main goals of Flanders' DRIVE is to stimulate innovative power in the automotive sector. To realize this,



between different suppliers is vital to ensure optimum cost-efficiency and maximum know-how. Flanders' DRIVE, a non-profit organization of Flanders-based automotive suppliers, takes up the challenge to strengthen all the forces. Five suppliers in the automotive industry founded Flanders' DRIVE in 1996: Bekaert, Bosal, BOSCH,

the organization wants to make specialist know-how and resources available through close collaboration between the companies and with research centers in Belgium and abroad. Flanders' DRIVE encourages proactive networking and information interchange between companies. It stimulates the exchange of technological know-how

through provision of advice and joint research and innovation projects. Furthermore, Flanders' DRIVE provides a forum for scientific research and technological development, through the Flemish Engineering and Test Center (VETC). VETC makes advanced test and engineering facilities accessible for local SMEs and dynamic starters.

Flanders' DRIVE will strengthen the product development capacities of the automotive suppliers and secure their competitive position in Europe and on world scale.

## EASICS NV joins the TranSwitch family

*IMEC and K.U.Leuven internationally recognized in providing excellent engineers.*



EASICS NV, located in Leuven (Belgium), was founded in 1992 as a spin-off from the Katholieke Universiteit Leuven and IMEC. Since its foundation, EASICS NV has specialized itself in the design of very complex digital chips for applications in telecommunication and digital signal processing. Recently, EASICS has become part of TranSwitch Corporation (Connecticut, USA). TranSwitch is a leading developer and global supplier of innovative high-speed

VLSI semiconductor solutions to original equipment manufacturers who serve three fast-growing end-markets: the worldwide public network infrastructure, the Internet infrastructure and corporate wide area networks (WANs). The acquisition of EASICS NV expands TranSwitch's capability with additional engineering talent, intellectual property and facilities.

EASICS NV will remain a separate Belgian company and will offer digital ASIC design services to

TranSwitch as well as other companies. By this acquisition, TranSwitch recognizes the important role that is played by the K.U.Leuven and IMEC in providing excellent engineers and the attractiveness of the Leuven region in Flanders.

For more information:  
<http://www.easics.be/>

## Industry link

### IMEC joins the ITEA-EUROPA project



IMEC recently joined the EUROPA (End-User Resident Open Platform Architecture) project. The project is part of ITEA (Information Technology for European Advancement) which is a collaborative industrial R&D program dedicated to strengthening software and software engi-

neering competence at European industrial level.

The objective of the EUROPA project is to exploit the full possibilities that the interactive Digital TV (DTV) system can offer to all the players in its delivery chain from content provider up to and including the consumer.

IMEC is leading the activity on the presentation of advanced content such as MPEG-4, VRML (Virtual

Reality Modeling Language), ... These activities mainly consist of the development of system-level QoS (Quality of Service) and transport of MPEG-4 content on an MPEG-2 transport and/or program stream.

IMEC and its EUROPA partners are also contributing to the definition of the new MPEG-21 standard.

## Patents

### Patents granted – 2 Q 2000

#### US

- Method for obtaining a high dynamic range read-out signal of a CMOS-based pixel structure and such CMOS-based pixel. (US 6011251)
- Method and apparatus for receiving and converting spread spectrum signals. (US 6038248)
- Emission microscope and method for continuous wavelength spectroscopy. (US 6043882)
- Method of programming a flash EEPROM memory cell array optimized for low power consumption. (US 6044015)
- Gastrointestinal probe (US 6006121)

## UCPSS 2000 - Fifth international symposium on ultra-clean processing of silicon surfaces

*Tutorial: September 17, 2000, Oostende, Belgium*

*Conference: September 18-20, Oostende, Belgium*

The UCPSS symposium, organized by IMEC, targets to increase the level of understanding on ultra-clean processing technology in all steps of IC production. The conference will address a broad range of topics, from general issues in ultra-clean technology to new areas of concern such as cleaning at the interconnect level, resist strip and polymer removal, cleaning and contamination issues for metallization, wafer backside cleaning and cleaning after CMP (Chemical-Mechanical Polishing). Prior to the conference, a tutorial will be organized on "Ultra-clean processing technology and general cleaning issues". This tutorial is intended to provide a short up-to-date overview of the relevant topics in this area.

For more information: E-mail: [info@timshel.be](mailto:info@timshel.be) <http://www.imec.be/6/6.5.html>



## 193-nm lithography workshop: SEA-ALASCA

*October 3, 2000, IMEC, Leuven*

On Tuesday October 3, the day before IMEC's Annual Research Review Meeting, an international workshop is organized by IMEC in collaboration with the European Commission (Semiconductor Equipment Assessment Program). The goal of the workshop is to disseminate the major results obtained in 193 nm on the ASML PAS5500/900 step and scan system, which has been evaluated extensively under the framework of an SEA project, called ALASCA (Advanced Lithography using ArF SCanner).

The target audience are lithographers and technology development managers.

For more information: <http://www.imec.be/193nm/>



## IMEC hosts HERMES and IEEE-VTC Events in October 2000

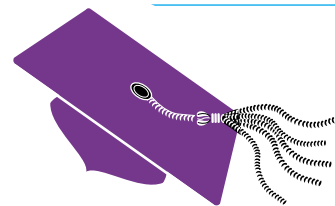
*October 18-19, 2000, IMEC, Leuven*



On October 18, IMEC hosts the HERMES Partnership Inauguration Event. The HERMES Partnership is the network of leading independent telecom research centers in Europe, in which IMEC plays a prominent role. Currently, the partnership counts 8 members. The secretariat and the Hermes manager are housed at IMEC. For more information on the HERMES Partnership or the Inauguration Event: <http://www.hermes-europe.org/>

The next day, October 19, the Communications Symposium 2000 of the IEEE-VTC Benelux takes place at IMEC. This event gives researchers from both industrial and academic environments a special opportunity to exchange experiences and expertise in all fields related to vehicular technology and wireless communications. The program includes keynote speeches by leading experts in the fields of interest and presentations of contributed papers. For more information, send e-mail to [ieee-vc@imec.be](mailto:ieee-vc@imec.be).

For more information: Cees J.M. Lanting or Marc Engels, IMEC, Tel: +32 16 281 211



## Researchers from IMEC, Cornell and MIT win 1999 Award for Excellence in Semiconductor Manufacturing and ESH

Two teams of researchers in environmentally benign semiconductor processing techniques won the 1999 SRC/SSA/International SEMATECH Excellence Award for Research in Manufacturing and Environment, Safety and Health (ESH). The award is shared by researchers of IMEC, Cornell and

MIT. Marc Heyns and Stefan De Gendt from the Ultra Clean Processing Group from IMEC received the award for their paper "A novel resist and post-etch residue removal process based on ozonated chemistries". Their research outlines environmentally friendly processes using ozonated DI water

to replace sulfuric acid-based processing in IC manufacturing. The process can be used for cleaning as well as removal of organic contamination, photo resist and organic post-etch residues from silicon surfaces.

## Marc Heyns receives the prestigious Werner Kern Award

The annual Werner Kern Award was established at the 1999 International Symposium to recognize and honor an individual or organization for their contributions to the development of new and innovative technologies for surface preparation. This award is given

out annually to a leading technologist. Last year's inaugural award was given to Werner Kern, known as "The Father of the RCA Clean", and one of the industry's technology forefathers. Marc Heyns received the award for his work on ultra-clean processing technology,

advanced gate stacks, thin dielectrics and epitaxial deposition of materials, as well as his work as author or co-author of more than 300 technical papers in journals and conferences.

## An Steegen wins the golden Graduate Student Award

An Steegen got the golden Graduate Student Award at the MRS Spring 2000 Meeting. This prestigious award is an international

appreciation of her work as a graduate student on silicide-induced stress in Si and its consequences for MOS devices. The work has led

to numerous publications and was carried out under supervision of Karen Maex (IMEC) and Paul Van Houtte (MTM KU-Leuven).

## IMEC receives best poster award on European Photovoltaic Conference

IMEC's Industrial Solar Cells group has been awarded the prize for best poster "Towards industrial

application of isotropic texturing for multi-crystalline silicon solar cells" on the 16th European Pho-

tovoltaic Solar Cell Energy Conference and Exhibition.



## Upcoming events

RADECS 2000 workshop	September 11-13, 2000	Louvain-la-Neuve (Belgium)
Fifth international symposium on ultra-clean processing of silicon surfaces	September 17-20, 2000	Oostende (Belgium)
193-nm lithography workshop: SEA-ALASCA	October 3, 2000	Leuven (Belgium)
Annual Research Review Meeting	October 4-5, 2000	Leuven (Belgium)
Hermes Partnership Inauguration Event	October 18, 2000	Leuven (Belgium)
IEEE VTC Benelux Communications Symposium	October 19, 2000	Leuven (Belgium)



How to write code for high-performance low-power multimedia applications?	June 26-29, 2000
General litho process training.	September 25-28, 2000
Low k1 training, including 193-nm lithography.	August 28 – September 16, 2000
C++ based hardware design of complex digital systems.	October 2-5, 2000
Silicon processing for ULSI circuit fabrication.	October 16-19, 2000
	November 27-30, 2000
	October 9-11, 2000
	October 23-26, 2000

For more information: <http://www.imec.be/>

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# Request for more information

n° **27** July 2000

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- Other: .....

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