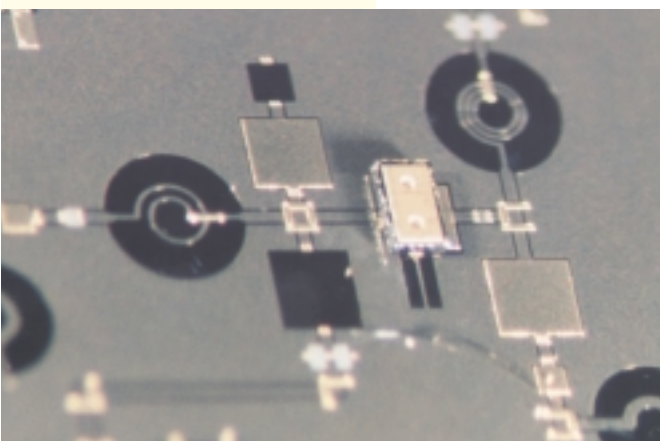


The past half-year was marked by the success of IMEC's consistent industrialization policy to support the Flemish industry. Three new spin-off companies were launched: FillFactory, Q-Star Test en Septentrio (more on page 8), IMEC collaborated in different initiatives to support the technological expansion in Flanders, and signed a license agreement with CS2. There is a growing awareness that development of next generation process technologies requires joint R&D. Several industrial partnerships were signed or initiated (more on page 6).

Integrated single-package receiver front-end



A microphotograph of the low noise amplifier

High-performance wireless communication systems require a high level of integration to reduce size and increase performance. However, single-chip integration of the analog front-end with embedded passives on Si is not yet feasible. Therefore, IMEC investigate single-package integration of complete transceivers based on a thin-film multi-chip-module technology (MCM-D) with integrated passives. IMEC has demonstrated a first single-package receiver front-end. The circuit was pre-

The integration of commercially available components with MCM (multi-chip-module) passives has been demonstrated for a 5 GHz WLAN receiver front-end.

sented at this year's IEEE International Solid State Circuits Conference (ISSCC).

continued p.2

Multimedia oriented data transfer pre-compiler (Acropolis)

IMEC developed a data transfer and storage exploration methodology to optimize global memory access, resulting in low power realization, low system bus load and better CPU performance.

Multimedia systems typically require a very large amount of data storage and transfers, causing high system costs. This is mainly due to

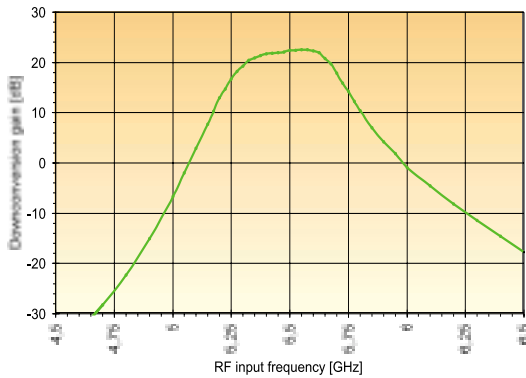
the large impact of the memory organization and the global data transfer on cycle count and system power consumption.

continued p.3

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Gain of the integrated receiver for a swept RF input frequency (IF = 500 MHz)

In a first step, a single-package receiver was integrated with commercially available bare-die components by using IMEC's in-house RF MCM-D technology. This technology allows to integrate at once stand-alone passive circuits, such as RF filters, and all the necessary passives for the active circuits. The in-

tegration of the band-pass filters avoids the use of discrete RF filters, which are still needed in 'single-chip' solutions.

The receiver incorporates two band-pass filters, a low noise amplifier (LNA) and a down-conversion mixer. It converts the 5 GHz RF input frequency down to an intermediate frequency of 500 MHz.

The low noise amplifier is built around a GaAs HEMT (high electron mobility transistor). The transistor is available as bare die and mounted with IMEC's flip-chip technique, avoiding high parasitics of bond wires. The down-converter is a GaAs MMIC (Monolithic Microwave Integrated Circuit). The two 5 GHz band-pass filters, which efficiently filter out neighboring distortions in the frequency spectrum, are located in front of the

LNA and between the LNA and down-converter. The complete receiver has a measured conversion gain of 22 dB and a noise figure of 7.5 dB. The integrated receiver measures 6.5 mm by 7 mm.

In a second step, the receiver front-end will be further developed by combining the MCM-D passives with custom designed ICs for the active circuitry (BiCMOS where possible, more adapted technologies where necessary). This will allow real chip-package co-design by making a good trade-off between on-chip realization or embedding in the MCM. A single-package approach has the advantage that it is not restricted to a certain technology, or to the availability or limits of commercial components, thus creating more degrees of freedom for design.

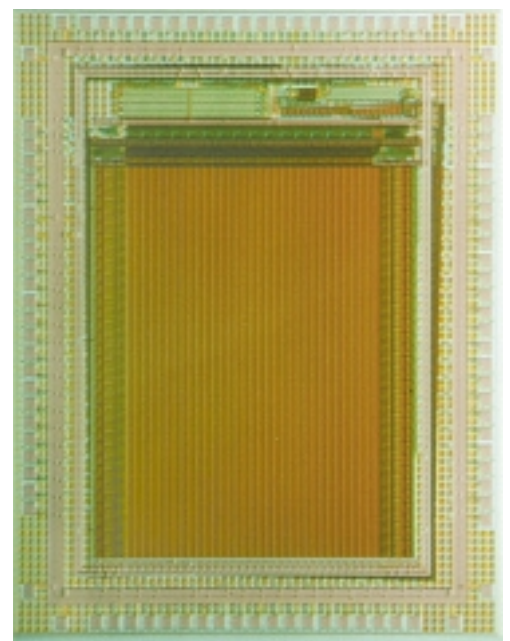
Technology report

1 Mbit HIMOS® Flash memory with 1 million program/erase cycles

The reliability evaluation of a 1 Mbit Flash memory, based on IMEC's patented HIMOS® technology, has revealed impressive endurance and retention results. While conventional embedded Flash technologies typically compromise in terms of performance, IMEC's solution exhibits 1 million program/erase cycles and more than 100 years of data retention. The 0.35µm HIMOS® technology adds only 30% to the cost of standard digital CMOS (5 additional masking steps) and yet exceeds the performance of other embedded Flash solutions. An interesting feature of this technology is that the

program and erase operations do not require any verification functions nor special algorithms on chip for obtaining these characteristics. Also the use of error correction code (ECC) is redundant in IMEC's solution due to the intrinsic robustness of the HIMOS® cell concept. This is the first time that IMEC has demonstrated the feasibility of the concept on such a large memory block, which was entirely designed and processed at IMEC's facilities.

1 Mbit HIMOS® Flash memory in 0.35 µm CMOS



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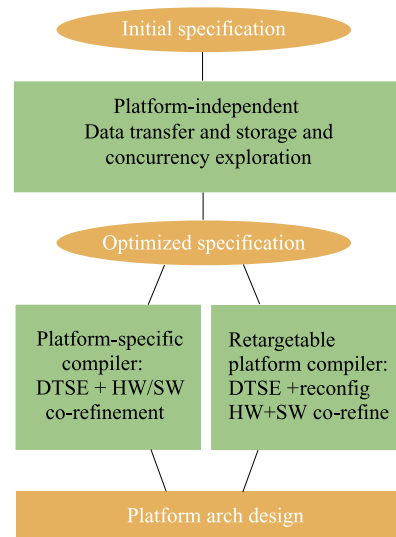
Therefore, IMEC has developed a DTSE methodology in a (parallel) multimedia processor context. The main objective was to reduce energy consumption, but recently, significant improvements have also been achieved in system busload and raw processor speed. IMEC's DTSE optimization is complementary to traditional compilers. It is a nearly platform-independent pre-compilation stage that can be used in front of a conventional compiler.

The platform-independence of the top-level steps of IMEC's approach has been clearly demonstrated for a medical imaging application, namely a cavity detection algorithm to detect brain tumors. For a single-processor context, very promising results on the combination of energy reduction and performance improvement, in both cycle count and system busload, have been obtained for this application running on a Pentium P2 with MMX support. After application of the DTSE approach, the

main memory/L2 cache data transfers are reduced with a factor 7.5. This heavily reduces both energy and system busload. Similar reductions have been obtained for the L1 cache transfers. After a subsequent application of the address optimization methodology to remove address overhead, the only remaining cycles are the minimally required ones. As a result, the pure cycle count is also reduced with a factor 3 compared to the conventional approach.

Similar improvements on performance, busload and power figures have been obtained on widely different processor platforms.

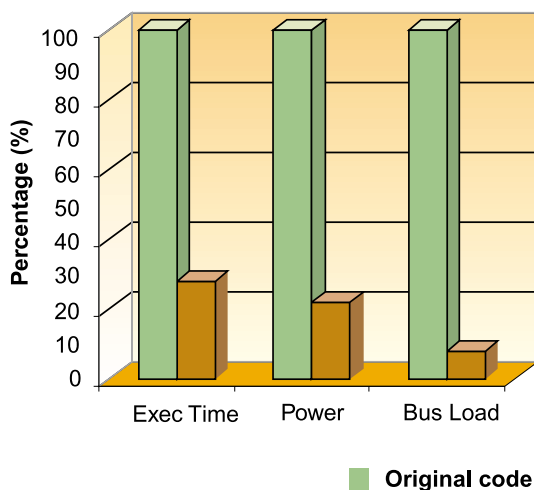
This desirable platform-independence is not fully true for the lower-level DTSE stages though. Here the memory organization parameters, like cache size and line size, number of ports and main memory bank organization, have to be incorporated to obtain really good results. For this purpose, a retargetable compiler is required to speed up the explo-



Systematic methodology for platform design with focus on DTSE aspects

ration of different memory architectures and different versions of the application code. With this DTSE pre-compiler the design time can indeed be strongly reduced in this stage. Around July 2000, IMEC is planning a release that will be available for help in the design of industrial multimedia applications, in the context of co-operations with industrial partners at IMEC.

Execution time, Power, Bus load (%)



Execution time on 4-way IBM SMP-Power PC 604 nodes

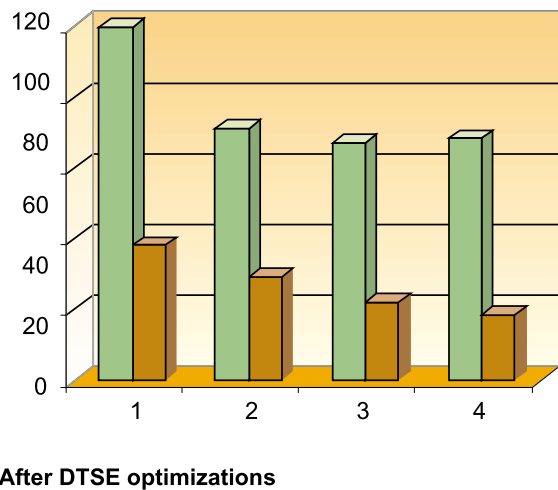


Illustration of platform-independent execution time, power and busload improvements for cavity detection algorithm

New construction techniques for sub-micron MEMS

IMEC patented the use of U-profiles in surface micromachining. The resulting mechanical stiffness enables the development of very thin micromachined actuators and sensors, such as uncooled bolometers.

Surface micromachining is a powerful and promising method for the fabrication of Si-based micro-electromechanical systems (MEMS). The basic processing concept is simple: first a sacrificial layer is deposited, patterned and etched to define the “anchor” points of the device. In a second step, the actual device layer is deposited on top of this sacrificial layer. Finally, the sacrificial layer is removed by etching, which results in a suspended device structure.

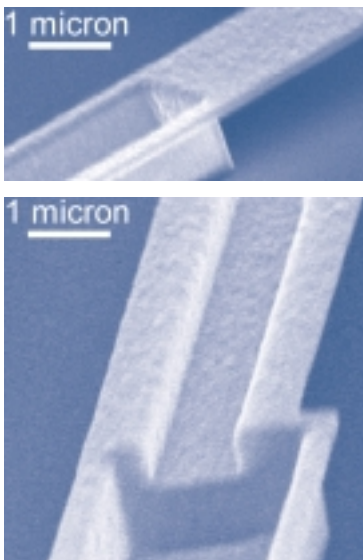
An infrared bolometer is a typical example of MEMS. Its operation

relies on a temperature rise of the resistive sensor. This can only be achieved by ultra-high thermal isolation. Infrared bolometers have previously been realized at IMEC using long supporting beams with sub-micron dimensions, consisting of a material with low thermal conductance such as polycrystalline SiGe. Although these sub-micron dimensions were routine in our pilot line, it was the first demonstration of sub-micron MEMS structuring. Ideally, the sensor and its support beams should be as thin as possible to maximize sensitivity and speed. However, this makes the sensor element extremely fragile, both during processing and during use. Any stress gradients in the composing layers cause bending of the device and leads to failure. To date, this has limited the material choice and minimal thickness for a host of surface-mi-

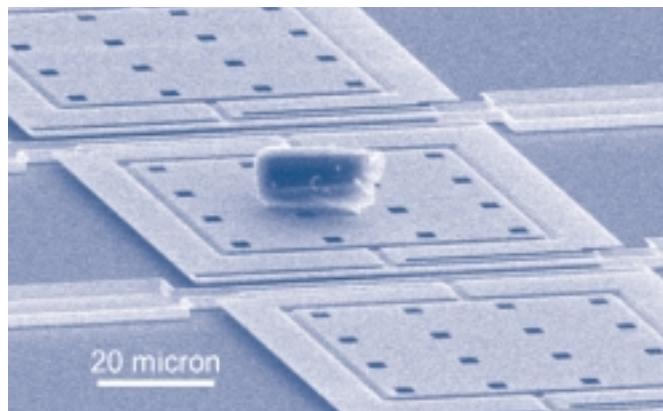
chromachined sensors and actuators.

IMEC has found and patented a fundamental solution to the above problems: U-shaped profiles. These profiles have very high mechanical stiffness at reduced weight and can be easily produced using surface micromachining. Compared to a solid beam with the same dimensions, the stiffness increases by up to three orders of magnitude.

This gain in mechanical strength allowed fabrication of very thin bolometers (as thin as 0.1 μm), which are still capable to cope with the destructive forces during the etch process and effectively solve the problem of residual strain gradients in the material. Furthermore, the thermal loss through the two support beams is even lower than the radiative heat loss of the sensor. The benefits of this new approach are evidently not limited to bolometers since increased stiffness is relevant for a large number of surface-micromachined devices.



Detail of a traditional support beam and its anchoring point (top) compared to the new U-shaped support beam (bottom)

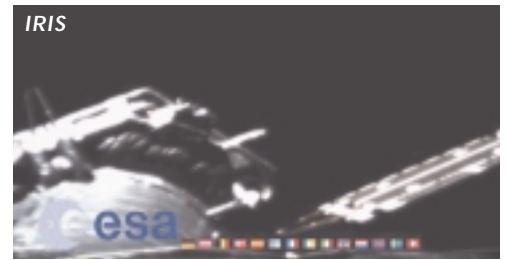
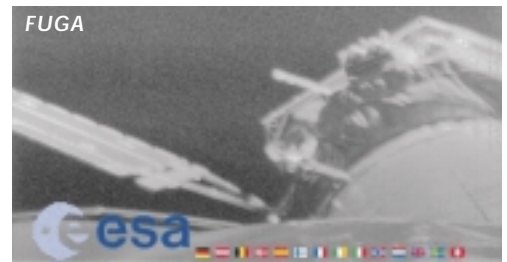


Suspended bolometer pixels featuring U-profiles in beams and sensor. Even accidental debris landing on the device (a lucky shot!) does not result in bending or failure of the device

CMOS cameras in space

The XMM spacecraft, launched on December 10 from Kourou, has taken pictures of itself in space. Two visual monitoring cameras (VMC) placed on the exterior of the spacecraft's focal plane assembly took the photographs. The cameras (10 x 6 x 6 cm) were developed by DSS/OIP and IMEC, and each weigh only 430 grams. The cameras verified the correct unfolding of XMM's large solar panels, and took unique images of

the craft's thrusters operated during manoeuvring. The cameras are of two types: FUGA and IRIS. The FUGA camera has a logarithmic response, with a high dynamic range, providing a black and white picture. The exposure time of the IRIS camera, used with color filter, can be modified. The field of view of both cameras is fixed, giving a view along the telescope tube towards the service platform and the solar arrays.



images courtesy of ESA/ESTEC

World's first SuperPON demonstrator

World's first SuperPON demonstrator realizes a 311 Mbit/s uplink and a 2.5 GHz downlink.



INTEC (associated lab of IMEC from the Gent University) developed a SuperPON (an optical-fiber ATM network) that supports up to 2048 network terminations over a range of 100 km, for both broadband and interactive access. This means several orders of magnitude improvement with respect to a conventional Passive Optical Network (PON). These improvements were achieved by using real-time switched optical amplification, combined with an innovating

Burst Mode Receiver (BMRX). The SuperPON offers a generic ATM broadband multiservice access at reduced cost, due to the physical concentration of all upstream communication, the statistical multiplexing, the dynamic bandwidth allocation and the consolidation of local exchanges.

The demonstrator works as follows: two Burst Mode Transmitters (BMTX) in two separate branches send bursts towards the BMRX, passing through 4 cascaded Semiconductor Optical Amplifiers (SOAs). Two SOAs per link are gain switched to handle time slots as short as 180 ns. This reduces the ASE noise and extends the dynamic range.

The new BMRX can handle weak signals in the presence of large varying ASE noise levels, and performs duty cycle correction. The sensitivity is -34 dBm and the optical dynamic range exceeds 12 dB, both tested in worst case condi-

tions. This SuperPON demonstrator proved a 311 Mbit/s TDMA uplink and a 2.5 GHz downlink. The system has been successfully demonstrated at the ECOC'99 conference in Nice (European Conference on Optical Communications, September 1999).



The SuperPON uplink experimental set-up

High-k dielectrics for deep sub-micron technologies

IMEC and ASMI collaborate on the development of Atomic Layer CVD technology for applications in advanced silicon device manufacturing.

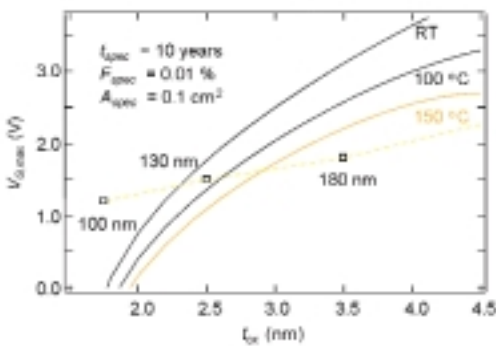
Scaling down the SiO₂ gate layer thickness in advanced CMOS devices is reaching its limits, both from the point of view of gate leakage current limitation as well as from intrinsic reliability. Recent IMEC research, indicates that be-

low 2.5-nm effective oxide thickness (EOT), the reliability of conventional thin oxide dielectrics is worse than previously expected. Consequently, alternative gate insulators with higher electrical permittivity than SiO₂ must be investigated for their potential applications as gate dielectric layers. The introduction of alternative gate insulators will be unavoidable for process technologies beyond 100 nm.

Development in such a critical layer in an IC is only possible through large-scale international collaboration. IMEC, in collaboration with its strategic partner ASMI, has set up an Industrial Affiliation Program to develop gate

dielectrics and gate electrodes for (sub)-100 nm devices. Within this program, IMEC wants to develop a manufacturable process for thin films (EOT < 1.5 nm) with low defect density and accurate thickness control.

IMEC and ASMI aim to use this technique to deposit very thin high-k dielectric layers, such as (but not limited to) Al₂O₃, ZrO₂, HfO₂, and their silicates for use as alternative gate dielectrics. In terms of deposition techniques, atomic layer CVD offers some unique advantages over competitive approaches. It results in perfect thickness and uniformity, as well as composition control over large substrates.



Reliability limit for thickness scaling

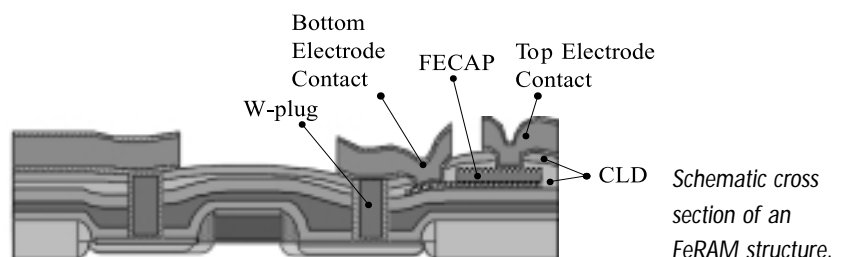
SBT ferroelectric memory cells

IMEC and STMicroelectronics collaborate in the development and integration of SBT (Strontium-Bismuth-Tantalate) ferroelectric memory cells.

The integration of ferroelectric memories with deep sub-micron technologies, becomes an attractive alternative for on-chip memories. New emerging applications, such as contactless smartcards, require low-power, fast programming speed and a large number of re-write cycles. Ferroelectric memories can offer such performance, as well as the potential for competitive cell size, cost and compatibility with sub-micron technologies. IMEC and ST have signed an agreement to jointly develop a ferroelectric SBT non-volatile memo-

ry module to be integrated into ST's current advanced 0.35 μm CMOS technology and compatible with more advanced processes in development. The collaboration will benefit from ST's experience in smartcard ICs and non-volatile, as well as from IMEC's work on inte-

gration and optimization of non-volatile memory based on the ferroelectric material PZT (lead-zirconate-titanate). SBT will be used as ferroelectric material because of its high endurance and superior voltage scalability compared to PZT.



Schematic cross section of an FeRAM structure.

Industry link

Philips and IMEC strengthen cooperation on IC process technology

Philips Research and IMEC have the intention to enhance their collaboration on research, development and integration of future process technologies. Philips will relocate a large fraction of its R&D on silicon process technology to IMEC. As part of the agreement, Philips will enter all process-oriented Industrial Affiliation Programs of IMEC and will use part of IMEC's pilot line for its own process research and for joint development.



The rapidly increasing complexity of IC process technologies and short time-to-market, increases the need for partnerships between companies and R&D centers such as IMEC. To further expand its technology competitiveness, Philips Research wants to combine its own expertise with that of another top research institute in this area.

Philips and IMEC collaborate already within several European programs, such as MEDEA and ESPRIT. Philips is also a member of IMEC's Industrial Affiliation Programs on lithography and ultra clean processing. It has decided to enter into a strategic alliance with IMEC for several reasons. IMEC is an independent research center and has a worldwide reputation as a re-

liable partner in technology R&D. In addition, IMEC has built up a worldwide expertise network with semiconductor companies, that allows joint and cost effective research.

This intended agreement will strengthen IMEC's position as leading independent R&D center in Europe. IMEC offers the skills and the infrastructure for developing sub-100 nm process technologies that Philips needs to cover the total silicon research activity.

Industry link

IMEC and Verteq sign agreement for single wafer technology

IMEC and Verteq, Incorporated have entered into an industrial partnership to implement a new drying technology into a single wafer cleaning tool provided by Verteq. As part of this agreement, Verteq has installed a Goldfinger megasonic single-wafer-cleaning module at IMEC. The tool features a new drying technology developed by IMEC. It will be used to develop improved single-wafer cleaning and drying processes for a variety of applications including copper post-CMP, and critical front-end cleans.



Goldfinger megasonic single-wafer-cleaning module

For more information see:
www.verteq.com

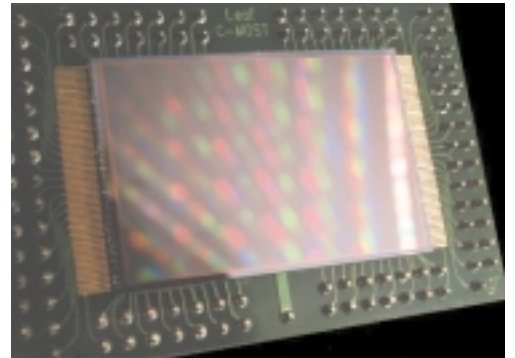


The new spin-off company FillFactory develops and markets new CMOS image sensors. These image sensors combine the high image quality of conventional CCD chips with the advantages of CMOS technology, such as lower power consumption and lower production costs. CMOS image sensors also render the possibility of integrating a number of electronic functions together with the sensor on one chip. The CMOS image sensor market looks very promising, and will enable totally new applications as portable videophones and Internet cameras.

IMEC has transferred a number of patented breakthrough technologies to its spin-off. In addition, the new company has taken over several international projects from IMEC and will also continue the development of CMOS image sensors for space applications, especially for ESA (European Space Agency).

The company's headquarters are momentarily based in Leuven. Their activities are focused on the development of customer-specific products for original equipment manufacturers and on the design, production and marketing of its own range of standard products.

In addition to IMEC and its founders, the shareholders include a number of Belgian (IT-Partners, Partner@Venture, Capricorn Ven-



CMOS active pixel sensor with 6.6 megapixels.

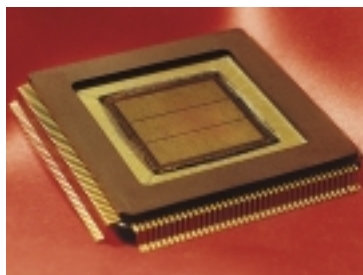
ture Partners) and international venture capital firms, including Prelude Trust Plc (UK), Sofipa (Italy) and Dow (Switzerland).

For more information, contact:
Lou Hermans, FillFactory NV
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B-3001 Leuven
Or send an email to
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Septentrio

satellite navigation

IMEC's latest spin-off company Septentrio develops and commercializes satellite navigation products. Septentrio provides in-house developed hardware and software blocks as well as complete satellite navigation systems. Their products are targeted towards the most de-

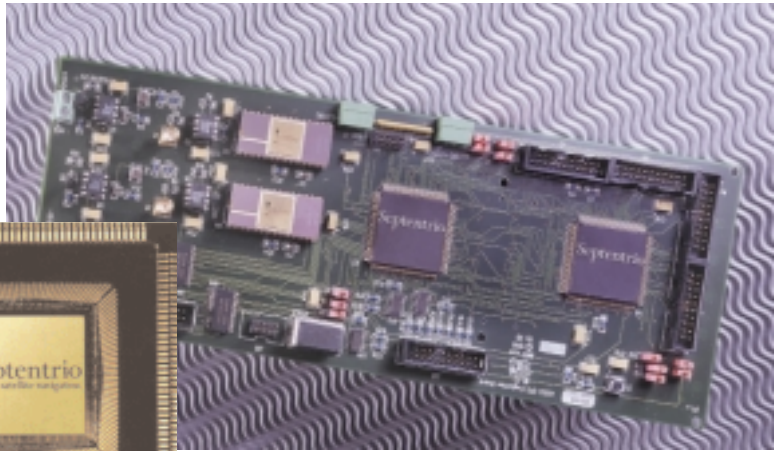
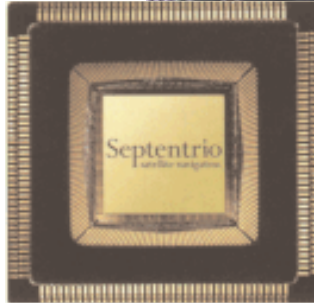


manding applications, such as marine and aviation navigation, precise timing determination, attitude determination and high-end consumer and automotive receivers.

The Septentrio technology is based on the GNSS Receiver Core, GR-Co®, an advanced and highly integrated baseband processor for all existing satellite navigation signals (GPS and GLONASS). Together with a microprocessor and radio front-end it allows to build a com-

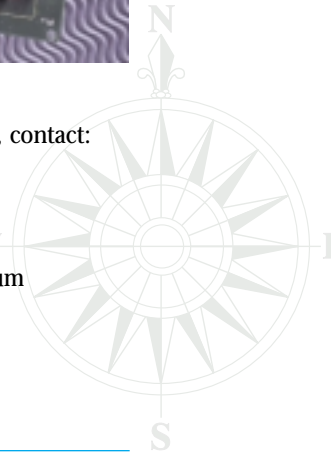
plete satellite navigation receiver, which can also process the emerging augmentation signals (EGNOS, WAAS and MTSAT). The GPS, GLONASS and augmentation capability offers superior accuracy, availability of satellites, and integrity.

The company's headquarters are still based in IMEC, Leuven. Their activities focus on the rapidly growing need for higher quality, more affordable satellite navigation products worldwide, and in particular in Europe. The company has emerged from IMEC's research program on satellite navigation. In addition



to IMEC and Septentrio's management and employees, the shareholders include IT-Partners, BizBees, Bayfield, Equinox Invest and private investors.

For more information, contact:
Peter Grognaard,
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Kapeldreef 75
B-3001 Leuven, Belgium
Or send an email to
info@septentrio.com



New IMEC spin-offs



THE CURRENT TEST COMPANY

Q-Star Test is a new spin-off company established by IMEC together with its associated laboratory, the higher polytechnic school KHBO (Katholieke Hogeschool Brugge-Oostende). The company commercializes new test methods for ICs based on supply current (I_{DDX}) measurements, for digital, analog and mixed signal applications. Testing of advanced integrated circuits becomes a real bottleneck

due to their increasing complexity. Therefore, there is an increasing interest in new test methods that allow efficient and fast qualification of ICs. Test methods based on supply current measurements is a promising alternative. Recently, there is a growing interest in I_{DDX} measurement solutions.

Test equipment builders will integrate I_{DDX} measurement modules in their test machines. Vendors of test pattern generation software will bring new products to the market that will support this test strategy.

Q-Star Test's headquarters are located in Brugge. The company offers I_{DDX} measurement solutions, consulting and training for auto-

mated test equipment (ATE) builders, test houses and ATE end users. The company also aims to provide consulting services for designers, to assist them in making their design I_{DDX} testable and to support the integration of built-in current monitors.

The shareholders are IMEC, KHBO, Creafund CVBA, Proseed Capital Holdings Ltd., Quadra Invest NV, MDV Consulting, ADP Vision and some private investors.

For more information, contact:
Hans Manhaeve, Q-Star Test NV
Konijnepijp 12
B-8200 Sint-Michiels, Brugge
Or send an email to
Hans.Manhaeve@Qstar.be

Leuven.Inc

Leuven Innovation Networking Circle



IMEC is one of the founding sponsors of Leuven.Inc, a new organization set up in 1999. Its mission is to create a regional network of knowledge intensive companies, and to stimulate technological and economical expansion in the region of Leuven. To reach this goal, the network wants to be a platform of communication that brings together local knowledge creators, by organizing special projects and events. At the same time, Leuven.Inc aims to stress the advantages of the area of Leuven as an essential junction of a global knowledge and network economy. Therefore, it wants to actively participate in the international network of the knowledge community.

For more information send email to: info@leuveninc.com

IMEC image sensors register popularity in Technopolis

Technopolis, the first Flemish “do center” on science and technology, was officially opened on February 26, 2000. The center is an initiative of the Flemish Government to bring science and technology closer to people.

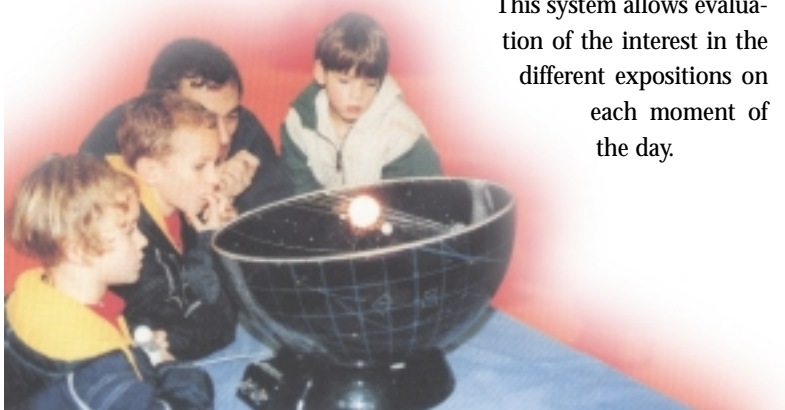
Technopolis starts from the familiar living environment and thrashes out the underlying scientific and technological principles. Visitors can learn the technologies from 227 different “do exhibitions” in a playful way.

An observation system was devel-



oped in cooperation with IMEC to assess the popularity of the different expositions. The sophisticated system is the first of its kind in the world. Several IBIS image sensors were mounted in the ceiling. The sensors are connected through an internal network and deliver color images indicating the number of visitors of each exhibition.

This system allows evaluation of the interest in the different expositions on each moment of the day.



IMEC licenses its advanced wafer-level thin-film technology to CS2

The Brussels-based semiconductor assembly and test foundry CS2 (Custom Silicon Configuration Services) makes its introduction to the stock market Easdaq. CS2 is a successful starter, founded in March 1998, and is in full expansion. It is the only European advanced chip assembly company.

IMEC has supported the company from its start, first through strategic alliance and in the fall of last

year through technology transfer. IMEC licensed its advanced wafer-level thin-film processing technology to CS2. The technology transfer includes flip-chip bumping, flip-chip redistribution techniques, wafer-level packaging, including thin film on glass, and high-density packaging technology with em-

bedded passives for RF front-end applications. These technology modules extend CS2's area array capability into higher value-added System-in-a-Package (SiP) solutions. SiP is the technology of choice for new generation electronic products for telecommunications and automotive applications. These products demand smaller size, higher system performance, better reliability and lower cost.



Industry link

IMEC offers deep sub-micron layout service for flip-chip packaging

Flip-chip mounting, using solder bumps, requires distribution of the input/output pads over the core area of the IC. To date, post processing of a chip, with normal layout for wire bonding, was needed to use the existing layout for flip-chip mounting.

Distributed area input/output is now integrated in the INVOMECE

back-end design flow for UMC 0.25 μm CMOS.

UMC 0.25 μm CMOS layout: I/O pads are distributed over the core area. There is a saving of 30% in silicon area, compared to normal layout for wire bonding



Industry link

European Commission funds EURO PRACTICE IC Service for the next 3 years

The EURO PRACTICE IC Service started 4 years ago by an initiative of the European Commission under the Esprit program. It was set-up to provide cheap CAD tools to European universities and low cost ASIC prototype and small volume fabrication to customers all over the world. The IC Service is offered by a consortium of five partners, namely IMEC (as coordinator), CLRC (United Kingdom), DELTA (Denmark), FhG-IIS (Germany) and Nordic VLSI (Norway). The European Commission has signed a new contract with IMEC and its partners, to fund the EURO PRACTICE IC Service under the IST (Information Society Technologies) program for another 3 years. The objectives are to further develop the service and to offer new CAD tools and IC technologies to European universities and companies.

During the past years, the service has developed to the world's largest and most advanced pro-

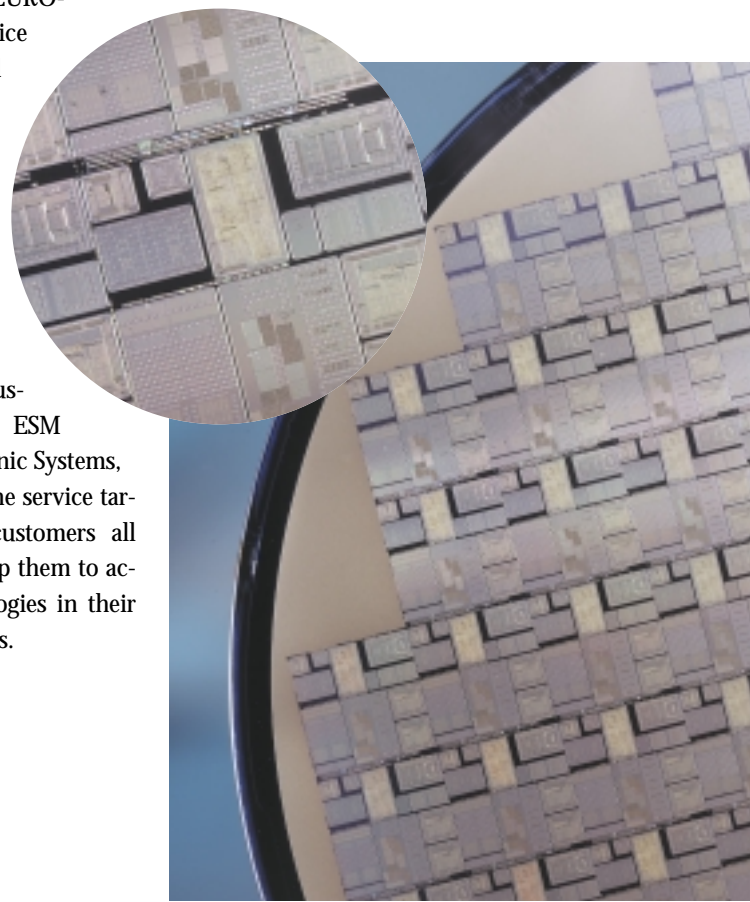
gram for the provision of micro-electronic tools for the research and training community. It gives academic and research laboratories in Europe the opportunity to undertake state-of-the-art research, training and interactions with industry, to enhance Europe's competitive position.

In addition, the EURO PRACTICE IC Service offers prototype and small volume fabrication in several technologies such as CMOS, BiCMOS, SiGe, GaAs and radiation hard technologies from foundries as Alcatel Microelectronics, Austria Mikro Systeme, ESM Ltd., Marconi Electronic Systems, TEMIC and UMC. The service targets mainly small customers all over the world to help them to access new IC technologies in their product developments.



EURO PRACTICE
IC SERVICE

For more information, please contact Carl Das – das@imec.be
tel: +32 16 281 248
<http://www.imec.be/europactice/>



MTC: Microelectronics Training Center

The growing shortage of people with the right skills has become a major road-block in the growth of the industry. That's why IMEC started a Microelectronics Training Center (MTC) to concentrate and expand its activities in dedicated training for industry, in the field of IC technology, ranging from design over process technology to packaging. Next to specialized courses for engineers, MTC organizes introductory ICT-oriented courses for non-specialists and non-technologists.

Training program

C++ based hardware design of complex digital systems

Introduction of concepts enabling the object-oriented design of hardware systems, using a C++-based design methodology and hands-on in using this methodology.

Scheduled on: 22-24 May 2000

25-27 September 2000

How to write code for high-performance low-power multimedia applications

Impact of source-to-source code-transformations and memory organization on cost and power consumption.

Application of these techniques to real-life multimedia and telecom applications.

Demonstration of emerging tools supporting the most tedious and error-prone steps.

Scheduled on: 26-29 June 2000

2-5 October 2000

Course in US: to be defined

Full custom layout

6-week course in cooperation with the local employment office on basic electronics, fundamentals in process technology and hands-on full custom layout.

Device reliability

4-day course on reliability of deep sub-micron technologies

Scheduled on: 18 and 25 April 2000, 5 and 12 May 2000

Silicon processing for ULSI circuit fabrication

State-of-the-art comprehensive training program in the practice, fundamentals, and emerging trends of silicon wafer processing for deep sub-micron devices.

Scheduled on: 23-27 October 2000 (under restriction)

Seminars on process technology and design

IMEC organizes weekly seminars on new developments in IC process technology and design. These seminars take place at IMEC and are also open to non-IMEC audience. A list and more details can be found on <http://www.imec.be/>



For more information,
please contact Bart De Mey
Bart.DeMey@imec.be
tel: +32 16 281 249
<http://www.imec.be/mtc/>



Events

Annual Research Review Meeting 2000

4 – 5 October 2000, Leuven, Belgium

Over the past 9 years, the ARRM has become a very dynamic, high-level platform with more than 300 participants last year. In this 2-day event, participants get an inside in IMEC's latest developments and evolutions in microelectronics. Next to the presentations, numerous possibilities are created for informal contacts and further discussions with IMEC staff members and other industrial participants. This offers a unique opportunity to explore common domains of interest and to obtain further first-hand information on strategies related to the challenging field of ICT. In addition, participants of the ARRM are kept informed, for one year, about important scientific breakthroughs at IMEC through its annual and scientific reports, newsletters and seminars. Due to the growing amount of participants, the ARRM 2000 will take place, for the first time, outside the

IMEC premises. Details, registration fee and location will be announced in April through the ARRM First Announcement. Do not miss this opportunity and request your personal invitation/ First Announcement now!



Conference contact: Mary Sroczynski
Events & Public Relations Officer - IMEC
Tel: +32 11 268 192 – Fax: +32 11 241 866
email: mary.sroczynski@imec.be
or visit the ARRM website: www.imec.be/6/6.1.html

Events

DATE 2000 – Design, Automation & Test in Europe

27- 30 March 2000, Paris, France

The DATE conference and exhibition is the main European event bringing together design automation researchers, users and vendors, as well as specialists in the design, test and manufacturing of electronic circuits and systems. The 4-day event consists of a conference with plenary keynotes, regular papers, posters, panels and tutorials as well as a commercial ex-

hibition. IMEC exhibits at DATE in Le Palais des Congrès at booth # 210. Come to attend live demonstrations in IMEC's embedded system village and learn more about our System-on-Chip design methodologies. On March 29, IMEC will bring a vendor presentation on design for the iHome (intelligent home): C++-based object-oriented system design, low-power

memory management, mixed signal analysis for reconfigurable WLAN and MPEG-4 multimedia. In addition, IMEC will give several lectures and hands-on tutorials.

For more information:
<http://www.imec.be/DATE/DATE.html>

booth # 210

SEMICON West 2000 Semiconductor processing and wafer fabrication

10-14 July 2000, San-Francisco, USA

booth # 4306

SEMICON West is the largest international exposition and conference dedicated to semiconductor equipment, materials and services in the world. Each year, more than 50,000 semiconductor professionals converge upon SEMICON West to network and exchange ideas and information on new and emerging products and technology.

SEMICON West 2000 will feature technical programs and sessions on the most critical challenges facing semiconductor manufacturers. IMEC will exhibit at SEMICON West in Moscone Center, Esplanade Hall.

Come to visit us at booth # 4306 and talk to IMEC's President & Vice Presidents, Research Direc-

tors, sub-micron pilot line experts, ... about IMEC's R&D activities, research strategy, new training initiatives, sub-micron process technologies transfers from IMEC to companies world-wide, IMEC's Industrial Affiliation Programs, ...

For more information:
<http://www.imec.be/6/6.html>

37th Design Automation Conference

5-9 July 2000, Los Angeles, USA

booth # 3462

The Design Automation Conference (DAC) is the premier Electronic Design Automation (EDA) and Silicon solution event. DAC features an outstanding technical conference with over 50 sessions led by leading system designers and researchers presenting the latest in design methodologies and EDA tool developments along with industry trends and information.

IMEC will exhibit at DAC in the Convention Center and will give different lectures during the conference. Visit us at booth # 3462 where you can attend our life demonstrations and learn more about IMEC's core competence in SoC design technology for integrated information and telecommunication systems. On July 5, IMEC will give an exhibitor pre-

sentation on design for the iHome: C++ based object-oriented design, low power memory management, reconfigurable hardware for WLAN, MPEG-4 multimedia, "smart appliances".

For more information:
<http://www.imec.be/6/6.html>

Other conferences with IMEC involvement

ISIF 2000, The 12th International Symposium on Ferroelectrics (ISIF)

12-15 March 2000, Aachen, Germany

EUROSIM2000, The first workshop on profiting from thermal and mechanical simulation of microelectronics

23-24 March 2000, Evoluon, Philips, Eindhoven, the Netherlands

The GOOD-DIE International Workshop - CAST2000

22-24 May 2000, Convention Center, Aix-en-Provence, France

4th European Workshop on Low Temperature Electronics

21-23 June 2000, ESTEC-ESA, Noordwijk, the Netherlands

2nd ENDEASD Workshop (European Network in Defect Engineering of Advanced Semiconductor Devices)

26-29 June 2000, Stockholm, Sweden

RADECS 2000 Workshop

11-13 September 2000, Louvain-la-Neuve, Belgium

For more information: <http://www.imec.be/6/6.5.html>

Awards



Hugo De Man receives Phil Kaufman award

Hugo De Man, senior research fellow at IMEC and professor at the K.U.Leuven (University of Leuven), received the EDA industry's most prestigious honor, the Phil Kaufman award. This award was created to honor those who make broad contributions to the industry and is annually bestowed by the EDA Consortium (EDAC).

Hugo De Man performed pioneering work in high-level languages and hardware/software co-design, which resulted in important changes in commercial EDA. Today, his interests have partly moved from the details of system-on-chip (SoC) design to the question of how to organize research and education for the SoC era.

Patents

Patents granted – 4 Q 1999 and 1 Q 2000

US

- Method for thermal impedance evaluation of packaged semiconductor components (US 5927853)
- Method for reducing fixed pattern noise in solid state imaging devices (US 5953060)
- Method of erasing a flash EEPROM memory cell array optimized for low power consumption (US 5969991)
- Contactless array configuration for semiconductor memories (US 6009013)
- A database and method for measurement correction for cross-sectional carrier profiling techniques (US 5995912)
- Method for obtaining a high dynamic range read-out signal of a CMOS-based pixel structure and such CMOS-based pixel (US 6011251)

Korea

- A method of producing a thin film transistor (KR 183964)

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Request for more information

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imec newsletter

I want to receive more information on:

- Integrated single-package receiver front-end
- Multimedia oriented data transfer pre-compiler
- New construction techniques for sub-micron MEMS
- High-k dielectrics for deep sub-micron technologies
- SBT ferroelectric memory cells
- IMEC offers deep sub-micron layout service for flip-chip packaging
- The EC funds the EURO PRACTICE IC Service for the next 3 years
- Other:

Please put me (or my colleague) on your mailing list for following publications:

- IMEC scientific report
- IMEC annual report
- IMEC newsletter

Name Phone

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