



Master Thesis/Internship

Topic Guide 2010-2011

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Information

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I. CMOS Scaling R&D

Atomic layer deposition for applications in nanotechnology

Atomic Layer Deposition (ALD) is an advanced technique to deposit thin films on a substrate from gas phase precursors. The film is deposited layer by layer through a cyclic process of self-limiting surface reactions. This technique allows growth control at the atomic level and deposition of extremely complex nanostructures.

ALD can be used for example, for improving the performance of computer chips and memory cells, by introducing novel materials, e.g. high-k dielectric oxides. A new potential application is energy storage in supercapacitors with nanostructured materials. ALD can also be used to increase the efficiency of solar cells, e.g. by introducing a passivation layer.

This topic fits in the research and development of ALD processes of metal oxides (e.g. Al_2O_3 , HfO_2 , SrTiO_3 ...) or metals (e.g. TiN, Ru ...). The ALD process parameters need to be optimized in order to achieve uniform (nanometer thin) films with optimized properties. For example, the self-limiting aspect of the surface reactions is examined as it provides the basis for the process control at atomic level. The deposition temperature can affect the amount of impurities in the film and its phase. For deposition of metal oxides, the oxidant precursor (H_2O , O_3 ...) also plays an important role. Insight in the surface chemistry (ligand exchange reactions or oxidation reactions) can provide a substantial contribution to the optimization of the process.

In order to characterize the nm-thin films, complementary measurement techniques are applied, such as spectroscopic ellipsometry, X-ray photoelectron spectroscopy, Secondary Ion Mass Spectroscopy ...

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in chemistry, physics, material science

Type of project: thesis and/or internship

Responsible scientist(s):

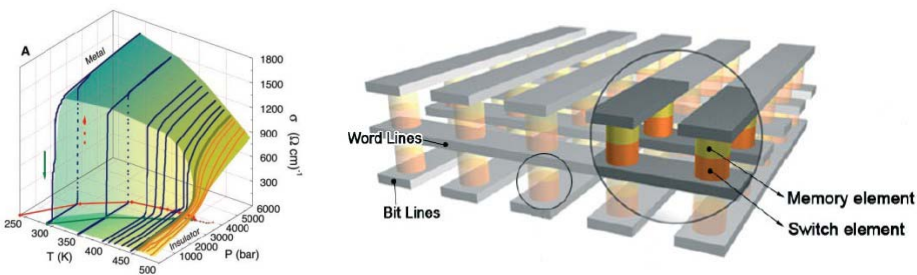
For further information or for application please contact Annelies Delabie (Annelies.Delabie@imec.be) and Sven Van Elshocht (Sven.VanElshocht@imec.be).

Tailored functional oxides for nanoelectronics

The downscaling in size of microelectronic components has led to the continued development of new products and markets: PCs, laptops, mobile phones, mobile internet... The main vehicle for this scaling, the MOSFET, is unfit to continue the downscaling trend beyond 5-10nm gate lengths. For flash memory it is expected that the downscaling cannot be extended because the charge used to store one bit should scale down to less than 100 electrons. At such low numbers, the information retention becomes problematic.

Electronic devices based on transition metal oxides are promising candidates for memory applications. Using functional oxides with tailored properties creates opportunities for new device concepts that allow continuing the scaling roadmap. Some of these oxides can undergo a Metal to Insulator Transition (MIT) which could be used as a switching phenomenon for memory applications. The MIT phenomenon occurs in materials with strong Coulomb repulsion between electrons and can be induced by a change in temperature, pressure or chemical composition or when an electric field or optical pulse is applied. The detailed understanding of the transition is lacking giving opportunity for scientific investigations of the phenomenon. At the same time, novel materials developed in this work could also lead to functional oxides for improved Resistive RAM (RRAM) devices.

The objective of the project is to incorporate functional oxides with tailored properties in metal-insulator-metal (MIM) capacitors for memory and field-effect devices for transistors. You will fabricate devices and develop device characterization methods. You will investigate the underlying physics of the MIT transition in these devices and the feasibility of using these functional oxides for memory applications. Depending on your interests, one or several aspects of this research can be incorporated in the thesis.



The MIT in V₂O₃

RRAM memory array

Degree:

Master in Science or Master in Engineering, majoring in physics, nanoscience, nanotechnology

Type of project: thesis and/or internship

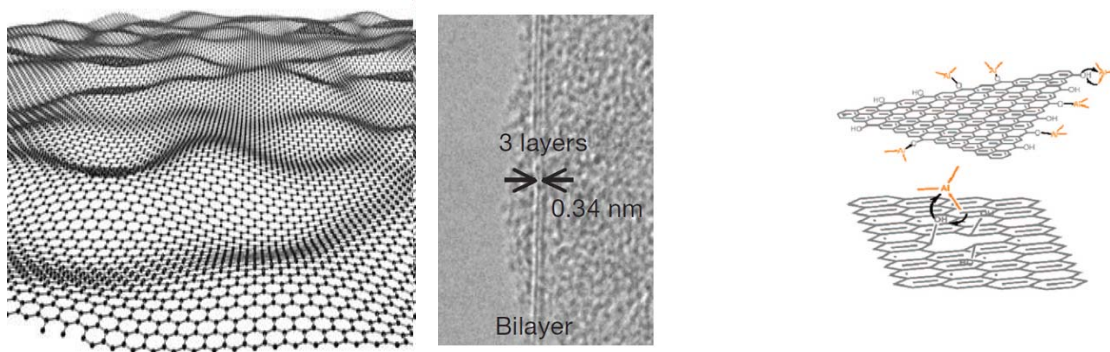
Responsible scientist(s):

For further information or for application please contact Koen Martens (Koen.Martens@imec.be).

Modification of chemical and physical properties of graphene

Nanotechnology needs innovative ways to harvest the properties of nanostructured materials into functional devices and new applications. Materials such as metals, semiconductors, oxides and even Carbon-based materials, exhibit novel electrical, optical and mechanical properties when shaped into nanosized dimensions. Only very recently, in 2004, a new type of nanomaterial based on Carbon atoms only, has been isolated for the first time.[1] This is the so-called graphene.

Graphene is a one-atom thick planar sheet of sp²-bonded carbon atoms that are packed in 2D honeycomb crystal lattice. Graphene can be considered as the basic building block for other sp²-carbon allotropes of different dimensionality, such as fullerenes, carbon nanotubes, and graphite. The peculiar electronic properties of graphene arise mainly from the energy band structure and the intrinsic low occurrence of defects and stiffness of its lattice. This makes graphene the thinnest carbon material that can show semimetallic behavior known to date.



The most promising aspect of graphene is that it allows changing the electronic properties at will by modifying its size, shape or surface properties. In combination with its high surface-to-volume ratio graphene shows a great promise in areas such as chemical sensing. Other interesting application areas are high-density nanoelectronics.

Theoretical calculations have shown that graphene “nanoribbons” can be used to fabricate field-effect tunnel transistors. Interestingly, these should outperform the switching properties of their Silicon-based equivalents.[2] However, to make such transistors, one has to shape the graphene as ribbons of a few nanometers wide.

In this project, you will fabricate graphene samples[3] and learn the basic techniques for fabricating prototype graphene devices. The work will start from earlier findings on graphene synthesis and surface modification experiments. During the project, chemical and physical techniques will be used to modify the surface properties of graphene in such a way that the electronic properties are influenced. Besides preparation and characterization of the graphene flakes, you will support device design and electric and optical characterization.

[1] S. Novoselov et.al., Science 2004 (306) 666.

[2] A.S. Verhulst, et.al., IEEE Electron.Dev.Lett, 2008 (29) 1398.

[3] A. K. Geim, P. Kim, Scientific American 2008 (4) 90.

Degree:

Master in Science or Master in Engineering, majoring in material science, physics, electrical engineering

Type of project: thesis or/and internship

Responsible scientist(s):

For further information or for application please contact Mirco Cantoro (Mirco.Cantoro@imec.be), Marleen van der Veen (Marleen.vanderVeen@imec.be) and Stefan De Gendt (Stefan.DeGendt@imec.be).

Study of the effect of VUV/DUV plasma light emission on polymer degradation

In a dry etch process, a substrate is exposed to a low pressure – low temperature plasma. The interaction of the surface with ions and neutrals lead to enhanced chemical reactions, and formation of volatile products/byproducts that desorb into the plasma. Those products are then evacuated through the pumping system, which ensure a continuous flow of gases into the chamber. Pattern definition is traditionally done by means of lithography, where a photoreactive polymer ('photoresist') is spun onto the substrate, and parts which have been exposed are developed and washed out. Remaining photoresist is used as a protection for the subsequent etch step, avoiding the underlying substrate to be attacked while the part exposed to the plasma is removed. In addition, the use of fluorocarbon-based plasmas usually leads to the deposition of so-called "plasma polymers", i.e. strongly disordered or amorphous CF_x films, that help building selectivity to underlayers ($SiO_2:Si_3N_4 > 10$, for instance) and photoresists. As a consequence, the patterning process, in terms of selectivity, chemistry, and especially roughness (LER=Line-Edge-Roughness), is strongly dependent on the plasma-polymer interaction.

In this work, we suggest to study the fundamental phenomena occurring when a polymer is put into contact with a plasma, principally focusing on the effect of VUV light exposure. Different types of polymers will be investigated: various generations of photoresists (365nm, 248nm, 193nm, EUV), and different types of plasma-deposited polymers (mostly fluorocarbon-based). Different type of plasmas, routinely used at imec (fluorocarbon plasmas, strip plasmas, post-exposure-treatments plasmas), will also be investigated.

By the use of various optical windows (MgF_2 , Al_2O_3 , SiO_2), we will try to separate the effect of ions bombardment from the effect of VUV/DUV exposure only. The polymer modifications will be investigated by various techniques, including ellipsometry (thickness, optical properties, film segregation, stress), mass (density), FTIR (bulk chemical modifications), AFM (surface roughening) and XPS (for some selected conditions). We will try to correlate those observations to the plasma emission properties, that be will be recorded by means of optical emission spectroscopy.

The topic involves theory, hands-on tool usage and wafer runs, analysis and data interpretation, and reporting.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in engineering, material science, physics, chemistry, ...

Type of project: thesis (5 to 6 months)

Responsible scientist(s):

For further information or for application please contact Jean Francois de Marneffe (marneffe@imec.be).

Metrology development for characterization of SiGe and Ge materials

In recent years, SiGe and Ge have become materials of choice for different applications in the microelectronics industry. The widespread application of SiGe and Ge is imminent and expected in the near future. Because of its low field mobility, Ge is used for high speed devices, and by mixing Ge and Si, (SiGe), the electrical properties of Si substrates can be tuned to obtain very efficient device performance. Expected to offer improved, more functional device operation in comparison with III-V element based devices, SiGe based devices are cheaper and their processing is relatively simple.

As a result of the growing application of SiGe and Ge in device production, there is an emerging need to develop functional metrologies to be implemented in processing these materials. Spectroscopic ellipsometry is a non-destructive, fast and reliable method used for the characterization of different materials, and it is widely used for in-line monitoring of various processes in production of semiconductor devices. This work will be focused on developing very accurate, ellipsometry-based metrology, for characterizing SiGe and Ge films after implantation and after dry and wet cleaning processing steps.

You will have an opportunity to work with state-of-the-art instrumentation, such as the microwave dry ash reactor and several spectroscopic ellipsometers in the imec cleanrooms. On top of the practical training, you can gain significant knowledge about different processes, such as dry ash processing and spectroscopic ellipsometry.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, chemical engineering

Duration of the project: preferably 3 months, starting March 2010

Responsible scientist(s):

For further information or for application please contact Dunja Radisic (radisicd@imec.be).

Effect of Ta, Ti, La and Hf contamination on Cl, Br, O and F radicals recombination

Further scaling in CMOS nano-electronics needs the combination of both new devices architectures and new materials. This brings a lot of challenges for all processing steps. Regarding the patterning process special care has to be paid towards metal based layers. Their removal and chamber contamination, due to their low volatility, have huge impact on reproducibility, uniformity and other process specification like critical dimensions, selectivity or profile control. This work is aiming to study the impact of the newest used metal layers on Cl, Br, O and F radical concentration. These radicals are being generated in different plasmas used for standard etch steps.

For this study we are going to use one of the most advanced etch chambers in 300 mm configuration. After a training period the student should be able to perform the etch and characterization by her/himself. At the end of the study there will be a possibility to publish the results or submit them to a conference.

We are looking for a person motivated to test his/her ability/skills in the amazing field of microelectronics.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, chemical engineering

Duration of the project: approximately 3 months, starting as soon as possible

Responsible scientist(s):

For further information or for application please contact Vasile Paraschiv (parasch@imec.be).

Patterning of TiN layer for Fin-shaped Field Effect Transistors (FinFETs)

Nano-electronics and nanoscience are relevant terms to describe the current trend in microelectronic device fabrication. These are linked immediately to nanometer size, which is the right word for the current technological nodes. Still, the current ongoing development requires also introduction of new materials and new device architecture in order to achieve smaller and smaller transistors. FinFET-based multigate devices are promising candidates for enabling the MOSFET scaling beyond 32 nm technology node. High-K/metal gate introduction over planar – FET goes one step further but beside the advantages brings also new challenges. From a patterning point of view removing the TiN layer deposited over the fin's without under etching it is very difficult if not impossible. Currently we are screening different etch chemistries to achieve this goal.

The purpose of this project is to develop such an etch process. Based on the available data the student will try to optimize the etch process. Understanding the etch mechanism is our final goal.

After a relevant training the student will perform the etch and characterization by her/himself. The etch and characterization tools are state of the art. At the end of the study there will be a possibility to publish the results or submit them to a conference.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, chemical engineering

Duration of the project: approximately 3 months, starting as soon as possible

Responsible scientist(s):

For further information or for application please contact Vasile Paraschiv (parasch@imec.be).

The effect of pulsed bias etching on the plasma etch process in an ICP Chamber

Plasma processing for dry etch purposes traditionally rely on a few basic parameters, allowing control of the discharge physics and chemistry: plasma power, substrate bias, flow of different gases, total gas flow, discharge pressure. In order to ensure a reliable pattern transfer, a basic requirement for the etch mechanism is to provide anisotropy. This means that patterned features usually need to be etched with vertical sidewalls, i.e. as little undercut/bowling/slope as possible. This can only be achieved by carefully tuning the plasma chemistry, and, by controlling the ion energy. For this purpose, a typical tool is an ICP chamber (Inductive Coupled Plasma), which allows the best separation between ion flux (driven by the so-called 'source power') and ion energy (driven by the bias voltage applied to the substrate).

Recent studies¹ addressed the question of using a cyclic process for optimizing the profile of deep (high-aspect ratio) contacts etched into SiO₂ with an amorphous carbon (\square -C) mask. In this work, the process was alternating between a no-bias deposition step (C₄F₆/CH₂F₂/Ar) and an etch step (C₄F₆/CH₂F₂/O₂/Ar) with high bias. They concluded that there were clear benefits on the profile of deep contact holes, suppressing the typical bowed shape observed usually with a continuous process.

With a pulsed substrate biasing, the self-bias voltage alternate between 0V (OFF state) and a finite value (ON state), leading to a mean ion energy varying between $e(V_p - V_i)$ and $e(V_p - V_{bias})$ where V_p is the plasma potential (positive w/r to ground), V_i the floating potential (slightly negative) and V_{bias} the self-bias voltage caused by the RF power applied to the wafer through a blocking capacitor (negative). Compared to a cyclic process, where the cycle duration is of the order of a few seconds, the pulsed bias process has a cycle duration which is much shorter, of the order of millisecond. Typical applied bias power is generated by a fixed 400kHz power supply, and the pulse frequency can vary between 100 and 2000 Hz. A second parameter defining the pulse shape is the duty cycle, with is equal to the period of the cycle during which the applied voltage is ON divided by the total cycle time (expressed as 10-90%, 100% is equivalent to the continuous process). Although deep Si via processes have been developed using this technology (Lam Research owned technology), little has been published on fundamental process understanding, i.e. influence of the pulse frequency/duty cycle on etch rates, film selectivities, polymerization curves for state-of-the-art processes. Prior art include work by Schaepekens and Oehrlein² and more recently by Raballand *et al.*³

The objective of this work is twofold: 1) first to understand the advantages of pulsed processing vs continuous processing, in terms of fundamental mechanisms driving the etch and selectivity of all specific layers each towards the other 2) second to determine how far a pulsed processing sequence (non cyclic, a priori) can be set up for the etch of advanced high-aspect ratio contacts, looking at issues related to CD, sidewall slope and stopping capabilities onto the Si₃N₄ "etch-stop" liner protecting the active devices from the etch process. More specifically:

1) First, we would like to develop a better understanding of the effect of driving frequency and duty cycles as a function of applied bias, for various materials used for current and future application, with a focus on "Through-Silicon-Via" (TSV) process and dielectric etch process (contact/via). From blanket etch rate tests on specific materials (SiO₂, porous SiOCH (BDII), SiC, etc...), we will study the way etch rate and the etching/deposition threshold evolve as a function of three main parameters (frequency, duty cycle, substrate bias). The discharge chemistries that we will investigate will be based on one hand on C₄F₈, C₄F₈-Ar and C₄F₈-O₂ gas mixtures (focusing on dielectric etch processes - SiO₂, SiOCH, SiC, \square -C and DUV PR), and Ar-SF₆ (focusing on Si etch processes - SiO₂, DUV PR, poly-Si or bulk Si). Eventually, plasma damage on porous SiOCH low-k may be studied, as it is known to be severely effected by processing in ICP chambers.

2) On a second hand, the blanket data will be used in order to study the applicability of the pulsed process for optimizing a deep contact etch process into SiO₂, by means of an APF mask. Comparison will be made between

¹ Cyclic Deposition/Etching Process to Etch a Bowing-Free SiO₂ Contact Hole, J.-K. Lee *et al.*, J. Electrochem. Soc. 156 (8), D269-D274 (2009)

² Effects of radio frequency bias frequency and radio frequency bias pulsing on SiO₂ feature etching in inductively coupled fluorocarbon plasmas, M. Schaepekens *et al.*, J. Vac. Sci. Technol. B 18(2), 856 (2000)

³ Porous SiOCH, SiCH and SiO₂ Etching in High Density Fluorocarbon Plasma with a Pulsed Bias, V. Raballand, G. Cartry and C. Cardinaud, Plasma Process. Poly. 4, 563-573 (2007)

the continuous and the pulsed processes, in terms of profile and process parameters (etch rate, slope). A cyclic process may be also considered. This part of the study will require some XSEM support and patterned wafers with state-of-the-art 193nm or DUV lithography.

- Timing for part 1) is estimated as 3 months, trainings (theory/tool/FAB) included;
- Timing for part 2) is estimated to 2-3 additional months, taking into account an additional training for XSEM or XSEM inspection through the SEM-support team.

Degree:

Master in Science or Master in Engineering, majoring in engineering, material science, physics, chemistry, ...

Type of project: thesis (6 months) or internship (3 months; then the package will likely be limited to phase 1)

Responsible scientist(s):

For further information or for application please contact Jean Francois de Marneffe (marneffe@imec.be) and Maarten Kostermans (kosterm@imec.be).

Characterization of amorphous carbon hard mask layers

Semiconductor device manufacturing makes use of lithographical processes to transfer a pattern into resist coatings to transfer this pattern further into the substrate by plasma etching. For patterns with typical dimensions below 65 nm, resist hard masks are wearing out during this etching. Therefore, the pattern is first transferred into another under-laying hard mask or 'advanced patterning film' (APF). APF layers are deposited in plasma enhanced chemical vapor deposition on 300 mm silicon substrates. The composition of these layers, adhesion and optical properties are important parameters in the device process.

This APF is composed of single (sp^3) or double (sp^2) bonded carbon atoms in the amorphous phase and can contain hydrogen and nitrogen. However, the exact composition of APF layers is thus far unknown.

The focus of this internship will be on the characterization of the composition of APF layers. This will be done by Fourier Transformed Infra Red (FTIR) spectroscopy, assisted by X-ray photoelectron spectroscopy (XPS) and Raman spectroscopy. The purpose is to link IR spectra to physical properties like optical absorption coefficient, atom density, conductivity and etching rate to obtain a deeper insight behind the controllability of deposition processes.

During this internship there is opportunity to make use of depositions performed in state of the art deposition tools inside the micro-electronic production environments. Several sophisticated tools can be used to evaluate layer properties and there are possibilities for scientific publication on the results.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, physics, chemistry, ...

Type of project: thesis with internship for a period of 6 months

Responsible scientist(s):

For further information or for application please contact Harold Dekkers (dekkers@imec.be).

Electrodeposition

Electroplating is one of the steps in producing chips and various devices, e.g. sensors. The wet-chemical deposition of metals is a reliable and cheap method for depositing metallization layers on a wafer and for filling through-silicon vias. During the processing of silicon wafers, various metals (mostly copper, tin, and nickel) are deposited. One of the challenges that lies ahead is to fill high-aspect ratio structures that are etched in the silicon wafer (typical structures are 50 – 100 μm deep and a few tens of microns in diameter). To obtain a reliable filling of these structures, various factors, such as additives in the plating solution, surface pretreatments and wet-chemical steps are being investigated. The research is part of the 3D program at imec, in which multiple active devices are stacked and electrical connections between the different chips are needed. This approach has the potential to increase chip performance, functionality, and device packing density. The student will participate in the work by doing experimental research. Possible subjects to work on are:

(1) Cu nucleation and growth

Before electrodeposition is done, a seed layer is vapour deposited, which is used to distribute the electrical current over the wafer surface. In vias, however, discontinuities in the seed are frequently observed, causing problems during electrodeposition. Therefore, an approach is required which is able to repair this. For obtaining a reliable filling process, the nucleation and growth of the metal deposit on various surfaces will be studied, using electrochemical measurements. Experiments on both flat and 'shaped' substrates will be done to get information about the conditions on the surface at the very start of metal deposition.

(2) Development of a method for visualizing defects in vias

Although the filling of vias is studied in great detail, quick and easy methods for characterizing the filling performance are lacking. Defects, e.g. voids, can be studied using techniques such as optical and scanning electron microscopy or electrical measurements. The goal will be to develop a new method that can be used to characterize filling performance of the vias. A wet-chemical approach will be investigated as a suitable option.

Degree:

Master in Science or Master in Engineering, majoring in chemistry, physics

Responsible scientist(s):

For further information or for application please contact Harold Philipsen (Harold.Philipsen@imec.be).

Direct electrochemical deposition of copper on liner materials for ULSI devices

Copper is used widely as metal interconnection in ultralarge scale integrated (ULSI) owing to its low resistivity and high reliability against electromigration. The present damascene copper interconnections are fabricated by electroplating on a physical vapour deposited Cu seed layer. Bottom-up fill of Cu using additives in acid electroplating solutions has been studied extensively. Although the electrodeposition process achieved the filling of deep and narrow trenches with copper, a few critical issues remain to be addressed, which include the need for a uniform sputtered copper seed layer, and the problem of non-uniform current distribution on the wafer. In recent years, seed-less copper deposition has been expected to be useful for the fabrication of ULSI copper interconnections. Nevertheless, direct plating on barrier in a conventional acid plating bath is very challenging in terms of initial copper nucleation density, fast-enough propagation of the copper plating front from the wafer edge to center, control of the first nanometers of the copper layer and of the uniformity.

The purpose of this work is to develop and characterize an alkaline direct plating chemistry that, due to the lower conductivity and different copper nucleation mechanism, is less dependent on the copper nucleation density and dependency on the position within the wafer.

The capability to achieve super filling of narrow features in the framework of the advanced interconnects will be explored changing the bath chemical composition at coupon scale.

The effects of chemistry and plating conditions on the deposition rate and super filling mechanism of the direct on barrier alkaline copper plating bath will be investigated by electron microscopic and focus ion beam observation of the cross sections of the trenches in patterned substrates and by deposition rate measurements on unpatterned substrates.

The primary objective of the project is to investigate and develop a plating process directly on the thin barrier layers.

You will test different commercial chemistries and benchmark with a model chemistry. Different barrier and seed layers, such as Physical Vapor Deposited (PVD) RuTa, Plasma Enhanced Atomic Layer Deposited (PEALD) Ru, Ta, TaN, Ti, TiN, Co, W are suitable candidates. The type of work proposed is fully experimental and an intensive use of the potentiostat for the electrodeposition tests is expected together with the preparation of the chemical solutions in the lab. Among other techniques, Scanning Electron Microscopy (SEM), Atomic Force Microscopy (AFM), X-ray Photoelectron Spectroscopy (XPS), X-ray diffraction spectroscopy (XRD), four point probe Sheet Resistance (Rs) measurement, four point bending adhesion measurement, are suitable candidates to be used for the characterization of the liner material and of the directly deposited copper layer.

Degree:

Master in Industrial Sciences or Master in Science, majoring in chemistry, chemical engineering, materials science, physics

Type of project: thesis or internship or thesis with internship, for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Silvia Armini (armini@imec.be).

“Seedless” electrochemical deposition of copper on liner materials for ULSI devices

An important step in the back-end of line processing of advanced microelectronic CMOS integrated circuits consists in laying thin copper interconnecting lines between active devices, such as transistors and capacitors. Copper lines are made by locally etching dielectric layers using plasmas through a patterned photoresist layer and filling the transferred patterns with copper. After the patterning, a very thin barrier layer to prevent copper diffusion into the underlying dielectric is deposited on top of the etched structure (e.g. Ta/TaN, TiN, CoWP, NiMoP, NiMoB). On top of the barrier film a seed layer is deposited which supports better adhesion of the Cu on the underlying material and acts as catalytic material during the electrodeposition process as well.

The relentless scaling of device geometry down to 32 nm-node technology and beyond, has introduced challenging metallization process requirements, spanning from void-free filling of nano-scale damascene features to the achievement of macro-scale uniformity across the wafer. In particular, the stringent requirements in terms of barrier and seed layer thickness reduction are a major concern for the subsequent plating process. Chemically-active thin seed layers, such as all the Cu-based films, needs careful cathodic protection to prevent sidewall voids, and trenches and vias are so small that they are filled with copper in just a few seconds. Thin seed layers are more prone to faster plating near the contact terminals at the edge of the wafer ("terminal effect") so that center-to-edge gap-fill uniformity becomes also a concern. In contrast with the case of chemically-active seeds, for chemically-inert substrates, such as Ru-based liners, instant center plating is not strictly required. Eventual defects, formed in the center of the wafer or at the sidewall of high aspect ratio features, can be repaired by subsequent plating directly on the Ru-based liners.

As a result, alternative strategies for the direct deposition of copper onto the barrier layer are required and will be the focus of the proposed work.

The primary objective of the project is to investigate and develop a plating process directly on the Ru-based liners. You will test different commercial chemistries and benchmark with a model chemistry. Different barrier and seed layers, such as Physical Vapor Deposited (PVD) RuTa, Plasma Enhanced Atomic Layer Deposited (PEALD) Ru, Ta, TaN, Ti, TiN, Co, W are suitable candidates. The type of work proposed is fully experimental and an intensive use of the potentiostat for the electrodeposition tests is expected together with the preparation of the chemical solutions in the lab. Among other techniques, Scanning Electron Microscopy (SEM), Atomic Force Microscopy (AFM), X-photon Spectroscopy (XPS), X-ray diffraction spectroscopy (XRD), four point probe Sheet Resistance (Rs) measurement, four point bending adhesion measurement, are suitable candidates to be used for the characterization of the liner material and of the directly deposited copper layer.

Degree:

Master in Industrial Sciences or Master in Science, majoring in chemistry, chemical engineering, materials science, physics

Type of project: thesis or internship or thesis with internship, for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Silvia Armini (armini@imec.be).

Optimization of resistive switching memories

In order to explore solutions to overcome the scaling limitations of conventional Flash memory cells, imec has started research activities on Resistive Random Access Memory (RRAM) cells.

Resistive switching memories are based on materials whose resistivity can be electrically switched between high and low conductive states. RRAM is becoming of interest for future scaled memories because of their superior intrinsic scaling characteristics compared to the charge-based Flash devices, and potentially small cell size (enabling dense crossbar RRAM arrays using vertical diode selecting elements). RRAM is seen as a potential candidate to replace existing memory technologies and hence to push memory technology towards the (sub-) 22 nm technology node. By the RRAM technology, people hope in the end to replace DRAM, SRAM, magnetic hard disks, DVDs, CDs, and so forth.

For making such RRAM, different concepts and materials are proposed. Imec's research activities on RRAM mainly focus on investigating the switching behavior of the RRAM cell concept that uses metal oxides as a switching element, and on demonstrating its scaling capability down to 25 nm. The research at imec concentrates on three main topics, being RRAM stack optimization (including the choice of top and bottom electrode and of the metal oxide), RRAM cell scaling and RRAM integration in a crossbar RRAM array.

The subject of the project is to develop new metal oxide materials. At first, you will be involved in depositing thin films of metal oxides (e.g. NiO, TiO₂, Ta₂O₅) using Chemical Vapor Deposition (CVD) or Atomic Layer Deposition (ALD), for which imec has acquired novel dedicated deposition tool. He/she will be participating practical work in the industrial-level 300 mm Clean-Room where the electronic structures are made and investigated using state-of-the-art fabrication and metrology instruments. The outstanding question to answer is how to quantify (modify) the oxygen and vacancy mobility and concentration in the metal-oxide thin films. The project will involve dedicated experiments to relate the chemical, physical and electronic properties of the circuits, in order to allow one to further optimize future resistive switching memories.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in materials science, physics, chemistry, electronics

Type of project: thesis or internship or thesis with internship for minimum 3 months

Responsible scientist(s):

For further information or for application please contact Johan Meersschaut (Johan.Meersschaut@imec.be).

Self-assembly of carbon nanotubes for NEMS applications

Nano electromechanical systems (NEMS) represent the intersecting domains of semiconductor processing technology and mechanical engineering at the nano scale. These are systems which have electronic functionalities and mechanical components strongly coupled to each other. Carbon nanotubes (CNTs) represent one of the best examples of nanostructures derived from bottom-up chemical synthesis. Due to their exciting electronic properties and mechanical robustness, CNTs have rightly been proposed as promising NEMS components over the past decade ^(1, 2). These properties can, for example lead to resonator arrays with very high resonance frequencies which would be ideal for wireless and sensing applications.

Currently, the biggest challenge to achieve such CNT arrays is the difficulty in controlling the horizontal position of CNTs on chip. The aim of this start-up work is to develop a self-assembly process based on the principles of dielectrophoresis (DEP) which can be used to position CNTs horizontally ⁽³⁾. With the help of localized electric fields, CNTs can be attracted locally to pre-defined electrical contacts, enabling direct post-deposition electrical characterization. A working model for a specific NEMS application (your personal ideas are encouraged here!) can be demonstrated with the devices obtained by the above method (also, depending on the time left in your thesis period).

The work involves getting familiar with working in imec's cleanroom; e.g. wetbench related chemical processing, using electrical set-ups like the wafer-prober for DEP and imaging systems like the SEM. The electrical characterization will be done in imec's measurement labs.

(1) H. Dai, Accounts of Chemical Research, 35, 2002, 1035-1044

(2) Hsin-Ying Chiu et al, Nano Letters, 8 (12), 2008, 4342-4346

(3) A. Vijayaraghavan et al, Nano Letters, 7 (6), 2007, 1556-1560

Degree:

Master in Science or Master in Engineering, majoring in chemistry, physics, chemical engineering, electrical engineering, materials science and engineering, nanoscience and nanotechnology

Type of project: thesis

Responsible scientist(s):

For further information or for application please contact Hari Pathangi (pathangi@imec.be).

Study of ultra shallow junction formation by Gas Cluster Ion Beam implantation and sub-melt laser activation

An important challenge for advanced Si Complementary Metal-Oxide Semiconductor (CMOS) technology is the formation of ultra-shallow source/drain extension junctions (USJs) with high dopant activation, high carrier mobility and low junction leakage. To comply with the stringent specifications for those USJs (see for instance <http://www.itrs.net>), novel doping and activation techniques are being introduced like molecular or cluster implants combined with “diffusionless” millisecond annealing.

The topic of this internship in particular will be the systematic study of n-type USJ formation by means of Phosphorous Gas Cluster Ion Beam (GCIB) implantation and subsequent laser activation. During GCIB processing, gas clusters of a few thousands atoms are formed and subsequently ionized/accelerated towards the sample (see Fig.1).

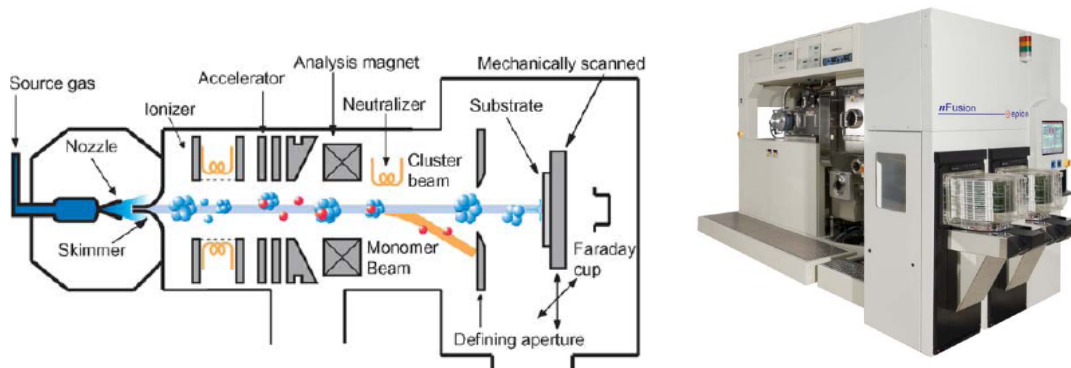


Fig. 1. Left : Schematic representation of the GCIB principle. Right : picture of a commercial TEL EPION GCIB system which is being installed in imec's 300 mm clean room.

Because of the low energy per atom and the localized energy deposition, multiple collisions occur near the surface inducing completely different irradiation effects from classical monomer ion beams. As a new GCIB system is being installed at imec, part of the work will be to explore and characterize the impact of different GCIB and annealing process parameters on the junction properties. To analyse the junction properties, a wide range of standard physical and electrical characterization techniques will be used (e.g. contact and contact-less sheet resistance measurements, micro-four point probe measurements, contactless leakage measurements, photo-modulated optical reflectance, Hall measurements, secondary ion mass spectrometry (SIMS), transmission electron microscopy (TEM), atomic force microscopy (AFM), etc ..).

The student will participate in the preparation of the samples in the 300 mm clean room and in the in-line characterization work. Besides the hands-on work, the student will gain insight in the mechanisms of cluster formation and assist in theoretical modeling to understand the observed trends.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in physics, electronics

Type of project: thesis or internship

Responsible scientist(s):

For further information or for application please contact Erik Rosseel (Erik.Rosseel@imec.be) or Jean-Luc Everaert (Jean-luc.Everaert@imec.be).

SiGeSn materials growth, characterizations and integration

GeSn/SiGeSn alloys present many interests in advanced technologies for both microelectronics and photonics purposes. Hole and electron mobility can be enhanced in advanced MOSFETs by using different integration schemes of GeSn alloys: within transistors channels or as Ge channel stressors in Source/Drain regions. Sn based alloys are moreover the only group IV materials having a direct bandgap allowing easy photonics implementation on Si substrates.

The purpose of this master thesis/summer internship is to investigate the properties and potentials of those new materials now in development at imec. GeSn materials growth will be mainly studied by using a lot of different characterizations techniques (RBS, XRD, Profilometry...) The student will participate to numerous discussions and will propose innovative solutions concerning such materials integration in both future microelectronics and photonics.

For this master thesis, a good knowledge of materials science is required. Skills in microelectronics and photonics are also a plus.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science

Responsible scientist(s):

For further information or for application please contact Benjamin Vincent (Benjamin.Vincent@imec.be).

The influence of surfactants on post-CMP cleaning processes

Chemical Mechanical Polishing (CMP) is a technique used to planarize a variety of circuit structures built on silicon wafers. A combination of mechanical polishing and chemical reactions at the surface gradually removes layers of deposited metals, oxides, nitrides etc. from the substrate. During this process, it is crucial to achieve a perfectly flat substrate in order to allow the fabrication of well-defined circuit components in subsequent process steps. CMP processes use a conditioned polishing pad and slurries to polish the surface, the precise characteristics depending on the particular substrate that needs to be planarized. The slurries usually contain both nanoparticles (as abrasives) and chemicals like oxidizers and inhibiting agents that assist in achieving an even polishing across the wafer without causing defects on the surface. After polishing, the substrate is cleaned extensively in a post-CMP cleaning step.

The post-CMP clean aims to remove all residue from the CMP process, which includes the slurry, chemical byproducts and the abrasive nanoparticles. In most cases all residue is removed in the cleaning step, leaving a clean and flat surface that is ready for further device-building. However, for some substrates and slurries, particles remain on the substrate and cause problems later on. The goal of this project is to use cleaning solutions containing surfactant molecules to remove left-over particles by using the affinity of the surfactant for the substrate. The surfactant will adhere to the surface and encapsulate the particles, which are then rinsed off. Ellipsometry experiments will show which kind of surfactant has the best cleaning capabilities for the studied substrate.

The project will focus on the study of particle-substrate interactions using in-situ ellipsometry with an impinging jet-cell located in the 200mm cleanroom. The setup allows the student to analyse the effect of experimental factors such as particle size, type and concentration of surfactant as well as cleaner flow rate on the aggregation of particles on the surface. The student is expected to run the experiments, analyse the results and to adjust further experiments accordingly. Additional analysis techniques will be used as deemed necessary. The results from the study will allow CMP process developers to improve the post-CMP cleaning step and significantly reduce the amount of residue.

Degree:

Master in Science or Master in Engineering, majoring in material science, physics, chemistry (basic knowledge of chemistry is a bonus but not required)

Type of project: thesis or internship

Responsible scientist(s):

For further information or for application please contact Lieve Teugels (Lieve.Teugels@imec.be).

Electrical characterization of MOS devices with novel channel materials (III-V/Ge)

With the 45 nm CMOS generation being in production, 32 nm CMOS in a pilot phase and process modules for 22 nm being worked on world wide, the end of the Roadmap for Si semiconductors is approaching very fast. One of the main limitations that Si is facing is its relatively poor carrier mobility. Even the shortest gate lengths cannot compensate for this anymore, and for this reason, the semiconductor industry starts to think about alternative materials that exhibit higher mobility and would allow making even faster circuits. An important candidate to replace Si, especially for pMOS transistors, is Ge. Very encouraging results about sub-micron pMOSFETs in Ge have been obtained at imec but, obviously, full CMOS needs also nMOS transistors, and there the high electron mobility of III-V compounds like InGaAs offers exciting possibilities. InGaAs as material is even more different from Si than Ge is and this asks for a lot of groundbreaking R&D work.

The candidate will participate in electrical measurements including CV, IV characteristics of MOS capacitors and transistors with Ge and/or InGaAs channels at various measurement conditions; investigating the impact of different process and physical parameters on the oxide-semiconductor interface quality as well as the transistor performance.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, physics, electronics, ...

Type of project: thesis and/or internship

Responsible scientist(s):

For further information or for application please contact Dennis Lin (dlin@imec.be) and Guy Brammertz (brammert@imec.be).

Evaluation of photoresist outgassing for Extreme Ultraviolet Lithography

Extreme Ultraviolet (EUV) light is currently of increased interest in semiconductor processing. EUV Lithography (EUVL) is the leading candidate for 22nm half-pitch device manufacturing and beyond. One of the concerns of this process technology is related to outgassing of materials in the vacuum environment – e.g. from photoresists –, which, enhanced by the EUV irradiation, can result in a reflectivity decrease of the optical elements and in other decrease of exposure tool performance.

In this field the student would work at imec on an experimental outgassing set-up (Fig. 1) to evaluate the EUV related outgassing. This is enabled by the RGA (Residual Gas Analysis) measurement capability which is integrated in this tool. It is the goal that the student is involved in outgassing analysis of various photoresist materials. This will contribute significantly to the understanding how materials and process conditions can impact contamination in the EUV scanners.

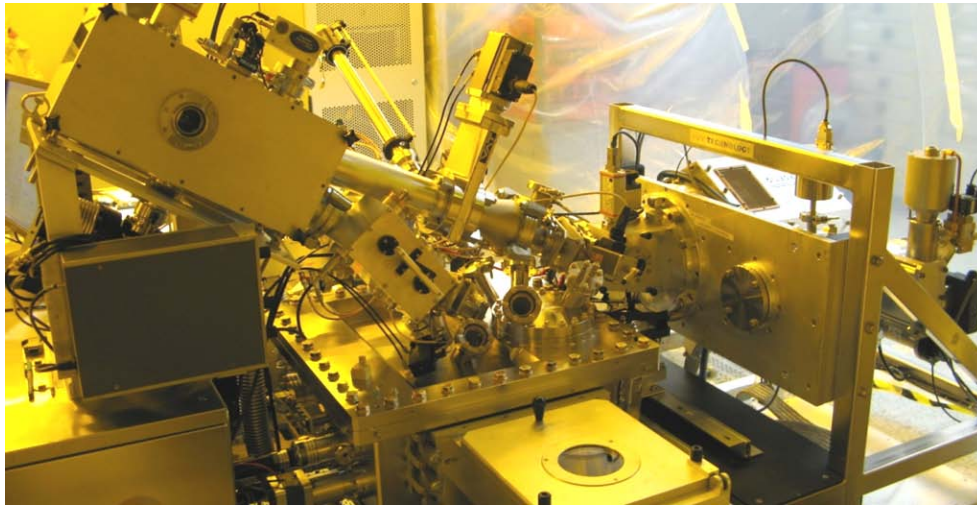


Fig. 1 : Experimental EUV outgassing set-up at imec for investigation of outgassing of lithography materials.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material sciences, physics, chemistry

Timing of the project: October-December 2010

Responsible scientist(s):

For further information or for application please contact Ivan Pollentier (Ivan.Pollentier@imec.be).

Automation of characterization of advanced microelectronic devices

With the downscaling of modern CMOS devices toward atomic dimensions, variation between nominally identical devices increases. Device parameters (e.g., the threshold voltage) need to be evaluated on tens of devices to collect sufficient statistics. Likewise, reliability (e.g., FET time-to-breakdown) and retention testing of non-volatile memories typically necessitates up to tens of hours per device. Characterization of modern CMOS devices therefore requires extended time and often consists of many repetitive tasks. To increase throughput and reduce user fatigue and error, such measurements need to be automated so they can run completely unattended.

The control software should be script-based to allow the user to assemble simple measurement sequences (e.g., “on a given set of devices, extract gate leakage and stress only devices with leakage below a given value”). The student will develop the software framework, including low-level libraries to control measurement equipment (e.g., a semiconductor analyzer or a robotic wafer prober) and high-level subroutines to perform electrical measurements (e.g., an I-V measurement) and to analyze data (e.g., extracting effective mobility). To increase throughput, the framework should allow for parallel measurements of multiple devices. The thesis work will be complemented by measurements and analysis of state-of-the-art imec devices. The applicant should be proficient in perl or python, should understand the basics of the GPIB protocol, and have an elementary notion about standard electrical measurements.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electrical engineering, computer science

Responsible scientist(s):

For further information or for application please contact Ben Kaczer (Ben.Kaczer@imec.be).

Characterization of metal-insulator-metal capacitors (MIMCAPS) for future DRAM applications

Future dynamic random access memory (DRAM) nodes require metal-insulator-metal capacitors (MIMcaps) with equivalent oxide thicknesses (EOT) ≤ 0.5 nm and low leakage current densities ($\leq 10^{-7}$ A/cm²). These technological specifications imply the introduction of high dielectric constant (K) materials in semiconductor fabrication lines. Alternative high-K materials with $K > 40$ typically have to be identified and integrated in MIMcap devices.

Imec, together with several industrial partners, has recently been very active in this field working on identification and screening of new high K materials as well as on the integration of potential candidates in devices. For example, several materials like SrTiO₃, BaZrTiO_x, Ba SrTiO_x and stacks are actively studied by physical and electrical characterization.

The future trainee will be working in the framework of this project. His/her main interest will be turned towards electrical characterizations of the candidates of choice. His/her work will also involve sample preparation, cleanroom work and stack definition. We are looking for a highly motivated person who wants to apply his/her fundamental knowledge to applied research and development project. The candidate has also to be ready to present his/her work in internal meetings when necessary.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electrical engineering, nanoscience and nanotechnology

Responsible scientist(s):

For further information or for application please contact Ben Kaczer (Ben.Kaczer@imec.be).

Positive/Negative bias temperature instabilities on ultrathin EOT (sub-1nm) logic devices

The continuous device scaling down allows the integration of a large number of transistors on a chip and increases the speed. One of the physical parameter reducing with the scaling is the equivalent oxide thickness (EOT). However, in thin dielectrics, BTI is known as a severe reliability issue limiting the scaling down. In thick high-k stacks with an EOT higher than 1nm, the dielectric consists of a (~1nm) SiO₂ interfacial layer between high-k material and Si substrate. Therefore, the methodology and the models built-up with SiO₂ dielectric are still applicable. In sub-1nm EOT high-k stacks, the interfacial layer is intermixed with the high-k and the first studies showed different degradation mechanisms compared to the thick EOT stacks.

In this study, both P/NBTI degradation mechanisms in very thin EOT regime will be investigated by exploring defects in the gate oxide. Also, the impact of the process conditions and different high-k stacks will be studied in order to optimize BTI reliability for thin EOT logic devices. A set of shift in drain current during bias stress at high temperature is a key characterization in this topic. For the applicant, a good knowledge of semiconductor physics is required. During the project, the student will have the opportunity to participate and interact with the researchers of the Logic/DRAM program.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, physics, electronics

Type of project: thesis and/or internship of minimum 6 months

Responsible scientist(s):

For further information or for application please contact Moonju Cho (Moon.Ju.Cho@imec.be).

Positive/negative bias temperature instability study on DRAM devices

The continuous device scaling down of Dynamic Random Access Memory (DRAM) devices needs devices with low threshold voltage (V_{th}). To achieve this goal, several methodologies such as ion implantation into the gate, or using rare-earth material capping layer are developed.

The aim of this proposal is to explore P/NBTI (Positive/Negative Bias Temperature Instabilities) reliability in the tuned V_{th} devices. A set of shift in drain current during bias stress at high temperature is a key characterization in this topic. And further study can be followed by charge pumping to figure out the interfacial trap density change. For the applicant, a good knowledge of semiconductor physics is required. During the project, the student will have the opportunity to participate and interact with the researchers of the Logic/DRAM program.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, physics, electronics

Type of project: thesis and/or internship of minimum 6 months

Responsible scientist(s):

For further information or for application please contact Moonju Cho (Moon.Ju.Cho@imec.be).

Evaluation of Cu contacts and reliability assessment of Cu diffusion barriers

In CMOS technology the transistors are connected through contacts to metal lines, which then join the individual devices to circuits. CMOS scaling is not only concerned with the reduction of the transistor dimensions such as channel length and channel width, but also the scaling of the transistor proximity. The down-scaling of the transistor contact size leads to a significant increase in the contact resistance. One possibility to reduce the contact resistance is to replace the conventional W-plug contacts by Cu contacts. First experiments show that this indeed improves device characteristics, but Cu diffuses very easily and hence a thin metal diffusion barrier is essential to avoid yield loss and reduced reliability. The total contact resistance depends on the material and the thickness of this diffusion barrier, and a tradeoff between sufficient barrier reliability and a low contact resistance has to be made.

The main task of this thesis/internship is the electrical characterization of Cu contacts. This includes the comparison of different diffusion barrier materials and deposition techniques, the evaluation of various newly designed test structures and the modeling of the contact resistance. Ideally after a training period the candidate will be able to work independently and under their own initiative. A general curiosity and interest in pursuing new findings is a definite advantage.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electrical engineering

Type of project: thesis or internship of 6 months

Responsible scientist(s):

For further information or for application please contact Thomas Kauerauf (kauerauf@imec.be).

Evaluation and reliability testing of transistors for DRAM applications

CMOS scaling is not only concerned with the reduction of the channel length and channel width, but also the scaling of other transistor parameters such as the gate dielectric thickness. The tunneling current through the dielectric increases exponentially with reduced oxide thickness and leads to unacceptably high power consumption for scaled devices. This is one of the reasons why high-k/metal gate stacks have been introduced and, depending on the application, these gate stacks are optimized either for high performance or low power consumption. The introduction of these new dielectric and electrode materials into a CMOS process is an enormous challenge because many compatibility requirements have to be met.

The main task of this thesis/internship is the electrical characterization of high-k/metal gate transistors for DRAM applications. This includes the comparison of different process splits such as dielectric material, layer thickness, deposition technique and post-deposition treatment. Ideally after a training period the candidate will be able to work independently and under their own initiative. A general curiosity and interest in pursuing new findings is a definite advantage.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electrical engineering

Type of project: thesis or internship of 6 months

Responsible scientist(s):

For further information or for application please contact Thomas Kauerauf (kauerauf@imec.be).

Evaluation and reliability testing of transistors with ultra-thin oxide thickness

CMOS scaling is not only concerned with the reduction of the channel length and channel width, but also the scaling of other transistor parameters such as the gate dielectric thickness. The tunneling current through the dielectric increases exponentially with reduced oxide thickness and leads to unacceptably high power consumption for scaled devices. This is one of the reasons why high-k/metal gate stacks have been introduced and, depending on the application, these gate stacks are optimized either for high performance or low power consumption. The introduction of these new dielectric and electrode materials into a CMOS process is an enormous challenge because many compatibility requirements have to be met.

The main task of this thesis/internship is the electrical characterization of ultra-thin oxide thickness high-k/metal gate transistors for high performance applications. This includes the comparison of different process splits such as dielectric material, deposition technique and post-deposition treatment. Ideally after a training period the candidate will be able to work independently and under their own initiative. A general curiosity and interest in pursuing new findings is a definite advantage.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electrical engineering

Type of project: thesis or internship of 6 months

Responsible scientist(s):

For further information or for application please contact Thomas Kauerauf (kauerauf@imec.be).

Study of the reliability of advanced nonvolatile memory devices

Conventional Flash memory technology (such as used in mp3 players, camera memory cards, ...) is very close to reaching insurmountable limits for further scaling and cost reduction. In order to overcome these limits, different improvements to the memory cell are currently under investigation.

Your goal in this thesis will be to study the reliability aspects of these improved stacks and memory cells (for example the use of engineered tunnel dielectrics or metal floating gates). Depending on the available material and interest of the students, other aspects can be studied.

On a practical level, this work would be mostly experimental, first characterizing the memory devices using state of the art electrical equipments and techniques, then trying to understand the behavior of the studied devices in order to decide on further optimization, evaluate the viability of the technology and eventually give suggestions how to improve the process and make better devices.

By the end of the work, you should be able to have an insight in the reliability behavior of the studied memory cells allowing to do suggestions on how to improve the device, and describe all the findings in a clear report.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electronics, nanoscience

Type of project: thesis

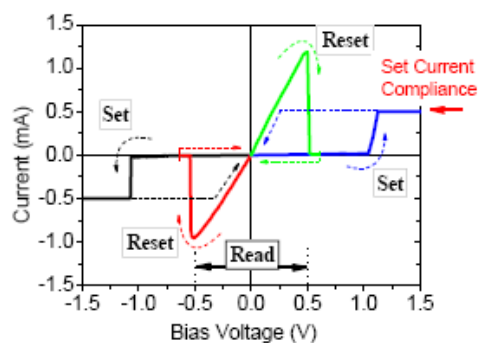
Responsible scientist(s):

For further information or for application please contact Jan Van Houdt (Jan.VanHoudt@imec.be).

Investigation of the mechanisms driving the resistive switching of NiO and HfO₂ RRAM memory cells

NiO films are known to exhibit resistive-switching properties, that is to say a change of its resistance level induced electrically. The figure below shows a typical I-V curve obtained for a metal/NiO/metal cell: initially in the high resistance state (HRS) the cell can be switched to the low resistance state (LRS) after applying a set voltage (V_{set}), and can be programmed again to the HRS state using a lower reset voltage (V_{reset}) of same polarity. This is referred to as unipolar-switching operation. The current understanding of the switching is that conductive filaments are created during the set programming, and disrupted during the reset programming. Unipolar resistive-switching was also observed in HfO₂ films sandwiched between metal electrodes, however involving probably different switching mechanisms.

Metal/NiO/Metal and Metal/HfO₂/Metal cells were prepared at imec, and show reproducible unipolar switching in DC switching mode.



Overall the physical mechanisms accounting for resistance switching is still unclear.

The purpose of the thesis work is to contribute to a better understanding of the thesis, by undertaking the following experiments:

- study the effect of different electrode metals on the switching and on the retention;
- study the effect of the cell size;
- carry out impedance measurements for different resistance states;
- study the switching at different temperatures (as from 70K);
- study the switching in different atmospheres (air, vacuum...), or after post-processing treatments.

Degree:

Master in Science or Master in Engineering, majoring in material science, physics, electronics

Type of project: thesis or internship of more than 3 months

Responsible scientist(s):

For further information or for application please contact Ludovic Goux (Ludovic.Goux@imec.be).

Study of the accurate measurement of sheet resistance and junction leakage on ultra-shallow semiconductor junctions

As CMOS devices get smaller with each technology node, the processes needed to fabricate and characterize these also become more and more complex. New fabrication processes for source-drain extensions typically involve low-energy cocktail or cluster implants (to obtain ultra-shallow junctions (USJs)), with or without Ge pre-amorphization, combined with flash rapid thermal or laser-based millisecond annealing cycles (to maximize activation while minimizing out-diffusion). Crucial technological parameters which directly relate to the performance of the final devices are the sheet resistance of the involved USJs and their junction leakage, which can be caused by remaining defects due to incomplete annealing.

Historically conventional four-point probes (with mm separation and 100 g load) have been used (and still are) for the determination of the sheet resistance. Recent work has, however, shown that only so called zero-penetration tools can reliably measure the sheet resistance of USJ's (i.e. avoid shorting through the underlying substrate). Two such tools are available at imec, i.e. the optical contactless RsL tool (from FSM) and the extreme-low pressure, micro-four point probe (M4PP) tool (from Capres using 10 micrometer probe separation). The RsL tool relies on the generation of a low injection of excess carriers (underneath a narrow mm-size light beam) which then drift outwards and generate a so called lateral junction photo-voltage (JPV) difference, which relates directly to the sheet resistance and junction leakage of the measured top layer. The RsL has, however, a poor geometrical resolution, i.e. centimeters. On the other hand, the M4PP can measure in localized areas (100 micrometer size), and also on structures where multiple junctions are present. It is, however, much slower than the RsL.

The goal of this work is to study systematically the complementariness of the RsL and M4PP tools on a series of state-of-the-art layers/structures with varying difficulties and to also build up a physical understanding for the observed differences. It has been observed, for example, that RsL fails frequently where M4PP remains accurate, possibly due to the presence of defects underneath the junction depletion layer. A theoretical framework is available for deconvoluting RsL data obtained on double junctions, but the latter still needs to be verified in practice (and might be of use in relation with the defectivity issue). Also other materials besides silicon, such as germanium or III-V materials are of interest, and need further experimental and theoretical work. For RsL, an existing simulation framework needs to be improved for new materials and the presence for defects. For M4PP, the impact of leakage current on the accuracy of the sheet resistance values needs to be studied. There is also an interest to measure with M4PP sheet resistances versus depth (along a beveled surface) to extract a carrier depth profile for sub-30 nm structures.

Degree:

Master in Industrial Sciences

Responsible scientist(s):

For further information or for application please contact Trudo Clarysse (trudo.clarysse@imec.be).

Development of a graphical user interface for a professional data simulation package for HRBS measurements

This will be the second part of a multi-year project aiming at the development and implementation of an integrated, professional software package in a graphical, object oriented, Microsoft Visual C++ programming environment (dialog boxes, menu's, toolbars, property sheets, etc.) for a completely new user interface for High Resolution Rutherford Backscattering (HRBS) measurements.

During the (past) first year the work was focussed on the incorporation of the essential basic graphical/computational modules into a user-friendly Windows-based integrated user interface in order to be able to convert the raw acquired data in to an appropriate data format. For portability reasons (towards Linux in the near future) this package has been developed based on the Trolltech Qt4 class library (opposite to MFC).

The focus of this second year will be on integrating a user-friendly simulation environment into the software. The main tasks will be as follows: (i) The first task will be to familiarize oneself with the existing software package, Visual C++ and Qt4, as well as with the basics of HRBS operation. (ii) To study an existing software package from Prof. Kimura (University of Kyoto, Japan) written in Quick Basic (QB), (iii) To make an object-oriented analysis of these QB routines and to integrate these QB routines in the Visual C++ environment, with an initial basic (simple) user-interface (for testing purposes), (iv) to visualize the output of the simulations and easily make overlays with experimental data, (v) to design and implement a highly user-friendly graphical user interface (among others using sliders for frequently changed parameters with instantaneous graphical updates) to interact with the routines from Prof. Kimura.

This subject is a challenge for those who wish to specialise themselves in all aspects and capabilities of object-oriented (Windows/Unix) programming within a Microsoft Visual C++ based environment.

Degree:

Master in Industrial Sciences, majoring in electronics/option ICT

Type of project: thesis (1 year) with internship (4 weeks)

Responsible scientist(s):

For further information or for application please contact Trudo Clarysse (trudo.clarysse@imec.be) and Bert Brijs (bert.brijs@imec.be).

Quantitative EDS analysis for materials characterization for nanoelectronics applications

During the development of new materials for nanoelectronics applications, quantitative analysis of dedicated test structures with small dimensions of 0.1-1 μm is often desired/needed. Established analysis technique usually used for composition/thickness analysis such as X-ray photoelectron spectroscopy (XPS), secondary ion mass spectrometry (SIMS), Rutherford backscattering spectrometry (RBS), and elastic recoil detection (ERD) lack spatial resolution in order to perform such localized analysis. Energy dispersive spectroscopy (EDS) has the possibility to analyze small areas as it is based on scanning electron microscopy (SEM) and is also used regularly for elemental identification. Quantitative analysis remains however often difficult especially for thin film analysis.

Imec is currently investigating the usefulness of EDS for quantitative thin film analysis within the framework of a collaborative project with an important EDS tool supplier. Results obtained during the first phase of the project look promising and therefore this project is focused on the aspect of quantitative analysis of bilayer thin-film systems, the exploration of two-dimensional analysis for several applications and the benchmarking with other techniques. A wide range of materials systems will be investigated in this project. The results of this work will provide clear answers towards the usefulness of EDS for localized analysis in nanoelectronics.

The student will work in a cleanroom environment and will be trained in the use of a SEM and EDS system. He/She will learn the basics of state-of-the-art analysis techniques and will closely interact with other members of the materials and components analysis (MCA) department.

Degree:

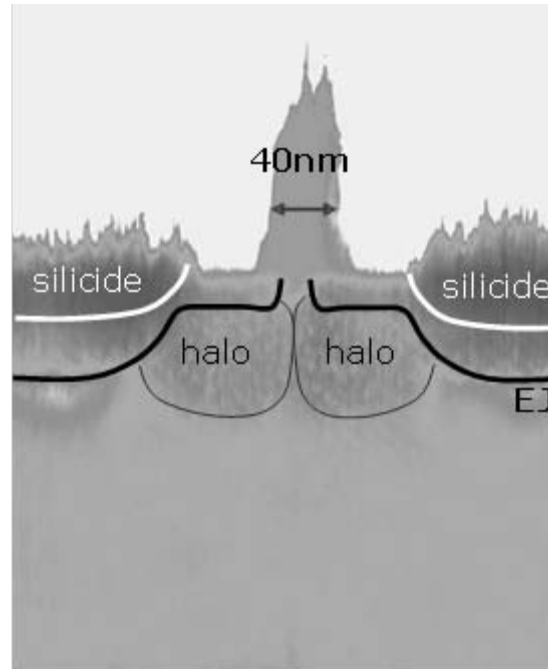
Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in physics, electrical engineering, material science, chemistry

Responsible scientist(s):

For further information or for application please contact Thierry Conard (Thierry.Conard@imec.be) and Thomas Hantschel (Thomas.Hantschel@imec.be).

Analysis and development of HV-SSRM

The SSRM technique is an AFM-based technique used to obtain 2D carrier maps of electronic devices (MOS, bipolar transistors, FinFets, nanowires,...) with (sub)-nm resolution. Samples therefore need to be cross-sectioned (polishing or cleaving). The latter may lead to artifacts such as Fermi-level pinning, surface states, native oxide,...



Recently a High Vacuum-SSRM version has been developed with improved performance relative to the ambient version, most probably due to reduced native oxide growth, contamination and anodic oxidation during the measurements.

In order to fully benefit from the vacuum, a more detailed understanding of the impact of the measurement environment is required as well as the role of eventual passivation procedures and cleaning/heating treatments after cross section preparation.

Task of the student(s) will be to study these effects and to correlate the electrical (HV-SSRM) performance with existing models for the high pressure SSRM-contact. The latter will involve studies on spatial resolution, ohmic contact formation (through studies of I-V curves), tip and sample erosion, and life time (re-growth, oxidation,..) of the sectioned surface.

Degree:

Master in Science or Master in Engineering, majoring in physics, electrical engineering, material science, chemistry

Responsible scientist(s):

For further information or for application please contact Pierre Eyben (Pierre.Eyben@imec.be).

Development of an industrial analysis-package in Visual C++2005 for SSRM-measurements

The goal of this project is to develop and to implement in the Microsoft Visual C++2005 programming environment a Windows XP software for the analysis of SSRM-measurements

SSRM (Scanning Spreading Resistance Microscopy) is a brand new technique developed a few years ago. SSRM makes use of a very small conducting probe (nm scale) to measure the local resistance of a small piece of conducting material along its cross-section. This delivers a two-dimensional resistance image where the colour of every pixel is corresponding to the measured resistance. The SSRM resistance picture has then to be converted as accurately as possible into a carrier concentration image where every pixel indicates the number of carriers (electrons and/or holes) present at every position.

This thesis is part of a long-term project (planned over a few years), which was started five years ago for the development of a completely new industrially oriented Visual C++ data treatment package. Two aspects will be investigated in this thesis:

- 1) Extension of an area-detection procedure towards new types of devices (e.g. FinFet, SOI, bipolar);
- 2) Improvement of a two-dimensional smoothing procedure for the resistance pictures (suppression of noise in the measurements) and of a two-dimensional quantification (from resistance to carrier concentration).

Degree:

Master in Science or Master in Engineering, majoring in electrical engineering, computer science

Type of project: thesis or internship

Responsible scientist(s):

For further information or for application please contact Pierre Eyben (Pierre.Eyben@imec.be).

Development of optimized procedure for backside analysis

The goal of this project is to develop and optimize sample preparation procedures for carrying out the analysis from the backside of a silicon wafer using X-ray photoelectron spectroscopy (XPS) and time-of-flight secondary ion mass spectrometry (TOFSIMS). Using these procedures, state-of-art semiconductor samples will be characterized. This work involves sample polishing procedures, optical microscopy and profilometry as well as atomic force microscopy (AFM). The student will learn the basics of XPS and TOFSIMS analysis.

XPS and TOSIMS are important analysis techniques in microelectronics technology for characterizing the composition of semiconductor samples. The analysis is commonly carried out from the wafer front side. As the advanced materials stacks have today often a thickness of only a few nanometers (e.g. for application in high-k metal gates), measurement artifacts are observed when the analysis is done from the topside. These artifacts can be overcome if this analysis is carried out from the wafer backside. For this, a total thickness of more than 700 micrometers of silicon must however be removed with nanometer precision. This requires an optimized polishing/etching procedure. Optical interference fringes can be used to stop the sample thinning at the desired thickness. For use as routine sample preparation method, an optimized procedure needs to be developed in this project. The optimized procedure will be used to characterize advanced materials stacks by XPS and TOFSIMS measurements.

The student will have to (a) develop lapping and polishing procedures for a backside-polishing tool, (b) optimize sample preparation procedures using gluing, polishing & etching, (c) evaluate the optimized sample preparation procedures on state-of-the-art materials stacks and characterize these samples by XPS and TOFSIMS.

The aspects that will be investigated in this project are (a) sample preparation: use of interference fringes as stopping layer during sample polishing/etching, (b) XPS/TOFSIMS: sample preparation versus analysis results.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in physics, electrical engineering, material science, chemistry

Type of project: thesis or internship

Responsible scientist(s):

For further information or for application please contact Thomas Hantschel (Thomas.Hantschel@imec.be).

Characterization of advanced nanostructures using a nanoprobe tool

Imec's nanoprobe combines a scanning electron microscopy (SEM) system, four nanomanipulation units and a parameter analyzer in one tool. Additional other components have recently been added to the nanoprobe such as an energy dispersive X-ray spectroscopy (EDS) unit, an electron beam induced current (EBIC) module and a micro-gripper which are extending the application range and allow for various manipulation, measurement and characterization tasks. It is used for example for electrically probing nanostructures such as nanowires and carbon nanotubes, for characterizing localized thin-film stacks, and for manipulating nanostructures using a pick-and-place approach.

The goal of this project is the further development of procedures for carrying out electrical measurements in an automated sequence. A basic software application based on the Labview programming language has been developed in the first phase and this software module will now be further developed and optimized in this project. The student will further improve the existing software program, implement additional features and will carry out electrical measurements on calibration and device structures. The student will work in a cleanroom environment and will be trained in SEM and nanoprobeing.

Degree:

Master in Science or Master in Engineering, majoring in physics, electrical engineering, material science, chemistry

Type of project: thesis or internship

Responsible scientist(s):

For further information or for application please contact Thomas Hantschel (Thomas.Hantschel@imec.be) and Pierre Eyben (Pierre.Eyben@imec.be).

Physical and electrical analysis of the buried metal gate – high k interface

The goal of this project is to use a recently developed sample preparation procedure (backside analysis) to study the interface of a metal-gate high k structure with X-ray photoelectron spectroscopy (XPS) and conductive atomic force microscopy (C-AFM). XPS is based on X-ray irradiation and the energy analysis of the subsequently emitted photo-electrons. As changes in chemical bonds/ environment are reflected in the energy of the photo-electrons, XPS is extensively used to probe material modifications and thus can provide information on the metal-high k material interactions as induced by the various processing steps. C-AFM is based on the atomic force microscope and uses a conductive tip to probe local (sub-nm scale!) variations in tunneling current through thin dielectrics. These variations can be translated into local electronic defects and contain information on material imperfections, trapping sites, trapped charges... As these methods have a very high surface sensitivity, one can not probe a buried interface like the metal gate - high k interface directly but needs to combine the actual measurement with some material removal. The latter is often done by ion beam sputtering from the top surface which however destroys the chemical bonds and thus the relevant information. Mechanical thinning of the gate layer would be an alternative but requires the ability to stop at 1-2 nm prior to the metal- high k interface (for XPS). Even in that case the C-AFM image will be totally dominated by the top metal layer and not reflect the dielectric properties. Removing the metal layer completely is not possible either as then the relevant interface is no longer present. To overcome these limitations an alternative approach is to work from the backside. Although ~700 microns of Si needs to be removed, one can use the silicon interfacial layer as a natural stop layer and end with the high k – metal interface entirely intact and close to the surface.

The sample preparation procedure for backside XPS-measurements has recently been developed and the objective of this thesis is to extend this further towards C-AFM as the quality of the final layer removal step is critical since any remaining Si-layer (even 1 nm thick) will totally shield the tunneling current. Prime emphasis of the work will however be on exploring the information which can be obtained from the backside XPS and C-AFM analysis when applied to a number of relevant cases based on metal gates – high k dielectrics (resulting from different deposition approaches and/or subjected to several process variations) and to correlate this information with macroscopic observations (Leakage, V_t , charge trapping,...).

The student will have to get acquainted with practical XPS-analysis (spectra collection, peak fitting), Atomic force microscopy and C-AFM (operation, I-V, I-t- mapping) and display fundamental insight in interpreting binding energy shifts (XPS) in terms of material interactions and I-V curves (C-Afm) in terms of electrical tunneling behavior.

Degree:

Master in Science or Master in Engineering, majoring in physics, electrical engineering, material science, chemistry

Type of project: thesis or internship

Responsible scientist(s):

For further information or for application please contact Wilfried Vandervorst (Wilfried.Vandervorst@imec.be).

Characterization of advanced solarcell structures using electrical atomic force microscopy techniques

Electrical atomic force microscopy (AFM) methods such as scanning spreading resistance microscopy (SSRM) and conductive AFM (C-AFM) are powerful and well established techniques for characterizing nanoelectronics device structures on the nanometer scale. SSRM measures the two-dimensional doping concentration by scanning a conductive diamond tip at ultra-high forces over the sample surface while measuring the local spreading resistance underneath the tip. In C-AFM, a metal coated tip is scanned at low force across the surface and probes local variations in tunneling current through thin dielectrics. These variations can be translated into local electronic defects and contain information on material imperfections, trapping sites and trapped charges. First experiments on using SSRM and C-AFM for studying doping profiles and grain boundaries in solarcell structures have shown promising results. This project aims on further exploring and optimizing the use of SSRM and C-AFM for solarcell characterization. One aspect of the work is the optimization of sample preparation steps for multi-crystalline silicon substrates using cleaving and polishing steps. The SSRM measurements focus on obtaining quantitative doping profiles and to correlate them to parameter changes in the fabrication process. C-AFM is used by the student to study grain-boundary and inter-grain defects. For this topic, the student will learn to operate an AFM system to carry out SSRM and C-AFM measurements. He/she will be part of imec's materials and component analysis (MCA) department and will also closely collaborate with members of the solar program.

Degree:

Master in Science or Master in Engineering, majoring in physics, electrical engineering, material science, chemistry

Type of project: thesis or internship

Responsible scientist(s):

For further information or for application please contact Thomas Hantschel (Thomas.Hantschel@imec.be) and Pierre Eyben (Pierre.Eyben@imec.be).

Development of a professional data analysis package for the micro-four point probe (M4PP)

The micro-four point probe (M4PP) is an electrical technique that allows for the very accurate measurement of the (sheet) resistance of a very thin (sub-100 nm) highly conductive semiconductor layer on top of a substrate of opposite impurity type (n- or p-type) (by pushing a current through the outer two probes and measuring the resulting voltage difference between the inner two probes). In 2009 such a M4PP tool has been installed at imec. The tool comes with commercial software (from Denmark) for the sheet resistance data collection, but not for the data manipulation of the many different data files or consequent data interpretation.

When applying this technique to a bevelled surface (slanted), one can generate a sheet resistance versus depth profile, from which the underlying carrier depth profile can be extracted. The latter is of crucial importance for the development of future state-of-the art transistors. There is, however, not yet any commercial software available to do this analysis in a user-friendly way.

The goal of this project is, therefore, to develop a completely new software package for both surface sheet resistance and carrier depth profiling analysis. The programming environment will be Microsoft Visual C++, with either the Microsoft Foundation Class (MFC) or the Trolltech Qt4 libraries. The major steps in this work will be: (i) Creating a user-friendly interface for loading all files (can be more than 100) from a single M4PP measurement folder, (ii) For surface analysis, making different types of result plots (resistance/voltage versus position, two-dimensional 200- and 300 mm resistance contour maps, etc.), (iii) For carrier depth profiling, smoothing the resistance data (using an available constrained cubic spline smoothing algorithm) and creating a user-interface for extracting the underlying carrier profile (choice starting point, entering bevel angle, choice of mobility curves), (iv) support making overlays with other profiles, (v) Eventually semi-automatically generate analysis results reports (in MS Word or PDF format).

It is not the aim of this work to develop new data treatment “algorithms”. This subject is, however, a challenge for those who wish to specialise themselves in all aspects and capabilities of object-oriented Windows programming within the Visual C++ environment with a multi document-view architecture (MDI) environment, focussing on a user-friendly graphical user interface (GUI).

Degree:

Master in Industrial Sciences, majoring in electrical/electronic engineering, option ICT

Type of project: thesis of minimum 6 months

Responsible scientist(s):

For further information or for application please contact Trudo Clarysse (Trudo.Clarysse@imec.be).

Carrier depth profiling with the micro-four point probe (M4PP) on advanced ultra-shallow CMOS semiconductor structures

As CMOS devices get smaller with each technology node, the processes needed to fabricate and characterize these also become more and more complex. New fabrication processes for source-drain extensions typically involve low-energy cocktail or cluster implants (to obtain ultra-shallow junctions (USJ's)), with or without Ge pre-amorphization, combined with flash rapid thermal or laser-based millisecond annealing cycles (to maximize activation while minimizing out-diffusion). Crucial technological parameters which directly relate to the performance of the final devices are the sheet resistance of the involved USJ's and the shape of their carrier depth profile.

Historically conventional four-point probes (with mm separation and 100 g load) have been used (and still are) for the determination of the sheet resistance. The Spreading Resistance Probe has been used for carrier depth profiling of USJ's on Silicon and Germanium and Electrochemical Capacitance Voltage on III-V materials. As new high mobility materials are, however, introduced and USJ become shallower (sub-50 nm), these conventional tools become basically useless (too high probe penetration, too large contacts, large correction factors, insufficient depth control, etc.).

A new promising tool to solve these problems is the micro-four point probe (M4PP). It has already been shown in the recent past that this tool can measure the surface sheet resistance very accurately with virtual zero penetration and is able to perform well on many types of new materials (SiGe, Ge, InGaAs, GaAs, etc.). *Hence, the main goal of this work is to develop a reliable procedure for the extraction of accurate sub-50 nm carrier depth profiles from sheet resistance depth profile measured along a beveled (slanted) surface on these new materials.*

The major steps in this work will be: (i) Familiarizing oneself with all the tools involved in this work (M4PP, profilometers, different polishing tools, software for carrier profiling, etc.), (ii) Optimizing sample preparation (polishing) for the different materials, (iii) Optimizing oxide deposition procedures for optimal starting point definition, (iv) Investigate the impact of different sensitivities (different probe pitches) and bevel angles (different measurement settings) on the accuracy of the extracted profiles, (v) correcting the carrier profiles for eventual artifacts (non-flatness bevel, insulating boundary effects), (vi) comparing results with other techniques such as Scanning Spreading Resistance Microscopy (SSRM) or Nanoprober data.

Degree:

Master in Science or Master in Engineering, majoring in physics, electrical/electronic engineering, material science

Type of project: thesis of minimum 6 months

Responsible scientist(s):

For further information or for application please contact Trudo Clarysse (Trudo.Clarysse@imec.be).

Study of Photo Modulated Optical Reflection (PMOR) on new high-mobility structures

Photo modulated optical reflection (PMOR) is a technique in which two separate lasers, a pump and a probe, are used. The modulated pump laser generates a high injection level ($> 1e18/cm^3$) of excess carriers in the investigated semiconductor structure and also causes a temperature change, both of which lead to variations of the underlying refractive index within the structure. The variations in reflected signal of the second probe laser, due to these changes, are then recorded and contain information about, for example, junction depth, peak carrier concentration, slope of the dopant depth profile, etc. At Imec two PMOR based tool, named Thermaprobe (using a modulation frequency of 1 MHz) and Boxer Cross (frequency of 1 kHz) are available. The former can measure offset curves (where the separation of the probe/pump laser beams is varied), the latter can measure power curves (where the power of the pump laser is varied).

Up to recently, all PMOR work at imec has focussed on silicon material. However, for the development of future technology nodes, there is a large interest in structures developed in germanium and/or InGaAs (III-V) materials. The last year an exploratory PMOR study on Ge/SiGe was made. *The goal of this work is to continue and extend this work further and to be able to present the final results at an international conference.*

This work will consist out of the following main parts: (i) familiarize oneself with the existing silicon and germanium related PMOR data and theory, (ii) Run additional experiments to complete the PMOR datasets for SiGe and pure Ge structures, eventually with measurements done outside of (KLA-Tencor in the US, or Semilab in Hungary) (using different offset ranges or wave lengths), (iii) Perform initial measurements on doped InGaAs layers., (iv) Develop a theoretical insight into the signals measured on these new materials, and how the signals can be used for junction depth determination, profile shape reconstruction, etc., (v) Extend the current Si-based simulation environment (using a device simulator named FSEM), to compare simulations based on the new theoretical insights with experimental data.

Degree:

Master in Science or Master in Engineering, majoring in physics, material science

Type of project: thesis of minimum 6 months

Responsible scientist(s):

For further information or for application please contact Trudo Clarysse (Trudo.Clarysse@imec.be) and Janusz Bogdanowicz (janusz.Bogdanowicz@imec.be).

Modeling backside illuminating CMOS imagers using TCAD software

Since the past few years, the technology of complementary metal oxide semiconductor (CMOS) image sensor has taken the place of charged coupled device's (CCD) technology in many applications. One of those being the space investigation, the developed imagers should exhibit very high quality properties in terms of high quantum efficiency, low crosstalk and high radiation tolerance. The Imager team in imec has been involved for the past years in that domain: backside-thinned monolithic and fully-hybrid CMOS active pixel sensors (APS) possessing excellent imaging properties have been successfully designed, fabricated and tested. In order to design and manufacture fully-hybrid CMOS APS possessing excellent imaging properties, different Technology Computer-Aided Design (TCAD) software tools were used. Those powerful tools are able to solve numerically complex physical equations and predict the performance of the device. Also critical microelectroning processing steps can be identified and optimized. Understanding the behavior of our current backside-thinned CMOS imagers and any further improvement requires different simulation models to be studied and developed.

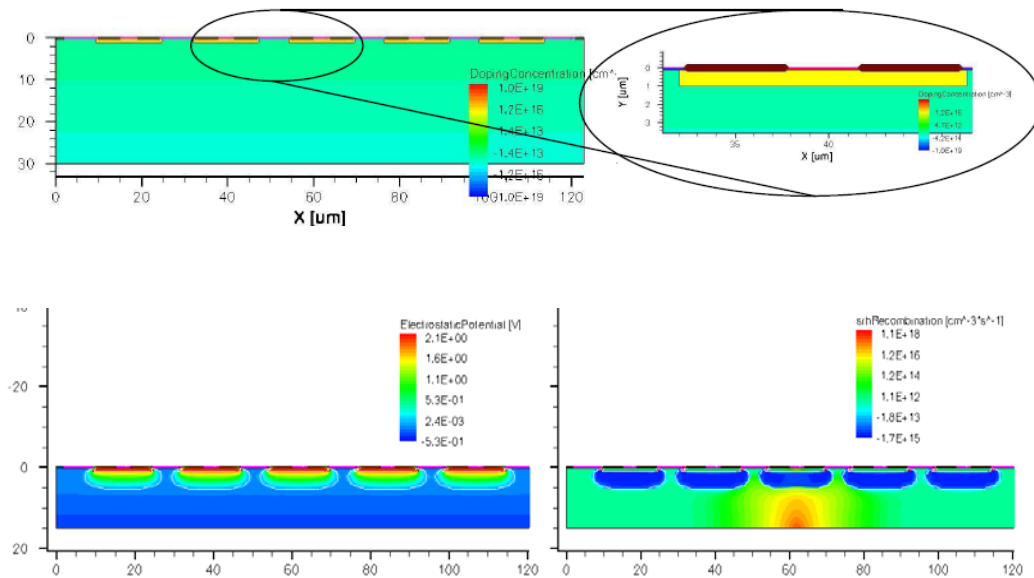


Figure: 2D array of five backside illuminated pixels (top) and simulated results of electrostatic potential and srh recombination (bottom)

The goal of this master thesis is to study physical mechanisms of the photodiodes, get familiar with the TCAD tool software, implement the physical models and the actual device design into the simulator and confirm the accuracy of the developed model by comparing simulations to measurements. Simulations can be done with existing software packages, Process and Device simulators of the Sentaurus Synopsis TCAD software. The student will start from existing CMOS imager models and will focus on specific improvements and modifications. The student will interact a lot with the Imager team at imec.

For this master thesis, you are expected to have a strong interest and/or background in semiconductor physics. Imec will provide training to UNIX/LINUX and to the device modeling techniques. Previous experience with the tools is not required. However, knowledge of TCAD software and/or physics of optoelectronic devices is an advantage.

Degree:

Master in Microelectronics or Master in Engineering, majoring in electrical engineering, physics

Type of project: thesis and/or internship for a period of minimum 5 months

Responsible scientist(s):

For further information or for application please contact Kiki Minoglou (minoglou@imec.be).

Characterization and removal of ion implanted photoresist

For the fabrication of different transistors on a chip, different regions of the substrate require different dopant concentrations. Therefore, a photoresist mask is used to block part of the substrate during the implantation of the dopant and hence protecting the transistors that require other dopants. However, during the implantation process, the resist polymeric structure is modified and a highly cross-linked top layer ('crust') is formed that can only be removed using aggressive oxidizing chemistries such as hot $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ mixtures or fluorine-based dry strip plasma chemistries.

These conventional resist strip solutions can no longer be used with further down-scaling of integrated circuits, because they are also quite aggressive towards the different materials present on the wafer and would result in unacceptable levels of substrate etching and/or oxidation.

In order to meet the very stringent requirements imposed by the semiconductor transistor roadmap on substrate loss, alternative strip solutions need to be considered to remove the resist.

The primary objective of this project is to develop selective wet-cleaning approach for removal of II-PR. For this purpose, in-depth characterization of the effect of various treatments on chemical and physical properties of ion implanted photoresist (II-PR) and its removal will be performed. The chemical modifications induced by the different treatments will be investigated using different analytical techniques such as Fourier Transform Infrared Spectroscopy (FTIR), X-ray Photoelectron Spectroscopy (XPS), contact angle measurements etc. The physical properties such as hardness and elastic modulus of the II-PR will be studied by nanoindentation technique. Finally, a mechanism of modification of II-PR by the different treatments needs to be built up. Based on it, a resist cleaning approach will be selected and optimized. The overall cleaning performance of the resist stripping process will be evaluated by optical microscope inspection and scanning electron microscopy (SEM).

In a second part of this work, the compatibility of the selected cleaning approaches with the other materials present on the wafer such as metal gate electrodes, high-k dielectric films and highly doped Si (or Ge) substrates need to be evaluated. Sub-nanometer thickness losses need to be determined using Spectroscopic Ellipsometry.

Degree: Master in Industrial Sciences, majoring in chemistry

Type of project: thesis for a minimum period of 2 months

Responsible scientist(s):

For further information or for application please contact Diana Tsvetanova (Diana.Tsvetanova@imec.be) and Rita Vos (vos@imec.be).

II. CMORE

Ultrasound imaging and power transmission Sources and receivers

Microelectronics experiences since the early seventies a period of sustained run-away development. Researchers strive to keep up with and fulfill Moore's law by scaling transistors down thus cramming always more circuits, more computing power and more functions on a chip always smaller and faster. However, this More of Moore era is said to be coming to an end.

The past decade has seen the start of a paradigm shift. Acknowledging the limitations of the scaling model for microelectronics, the emergence of novel technology drivers and appearance of new usage scenarios, e.g. low power, nomadism, health care and health monitoring, ..., researchers started exploring alternative technological paths. This defines the so-called More than Moore approach that departs from the one technology fits all approach and aims at developing a plurality of diverse ad-hoc technologies and according interfacing solutions. RF-MEMS is one of these technologies.

High-frequency MEMS resonators are the basic building blocks for embedded ultrasound systems. With their high Q-factor, high-level of integrability, MEMS devices allow to define arrays of ultrasound sources and receivers on-wafer, with their CMOS drivers and readouts. Besides the obvious extension of the well-known concept of echography, such systems are promising alternative solutions for example to the problems of in-vivo power delivery to implanted devices.

The objective of this project is to design and characterize MEMS-based ultrasonic sources and receivers. These devices will have to be optimized for example for power-delivery. Major attention will be laid on the isotropic power-scavenging ability of the receiver and increased directivity of the source obtained through appropriate arraying. Required simulations will be performed in COMSOL and/or ANSYS (with hands-on training).

Degree:

Master in Science or Master in Engineering, majoring in physics, electronics, mechanics

Type of project: thesis or thesis with internship

Responsible scientist(s):

For further information or for application please contact Xavier Rottenberg (Xavier.Rottenberg@imec.be).

MEMS/NEMS acoustic devices and circuits

Microelectronics experiences since the early seventies a period of sustained run-away development. Researchers strive to keep up with and fulfill Moore's law by scaling transistors down thus cramming always more circuits, more computing power and more functions on a chip always smaller and faster. However, this More of Moore era is said to be coming to an end.

The past decade has seen the start of a paradigm shift. Acknowledging the limitations of the scaling model for microelectronics, the emergence of novel technology drivers and appearance of new usage scenarios, e.g. low power, nomadism, health care and health monitoring, ..., researchers started exploring alternative technological paths. This defines the so-called More than Moore approach that departs from the one technology fits all approach and aims at developing a plurality of diverse ad-hoc technologies and according interfacing solutions. RF-M/NEMS is one of these technologies.

Acoustic devices, e.g., resonators, transmission lines, filters, ..., are key building blocks for future telecommunication systems. Indeed, with their extremely high Q-factors and linearity, these devices promise making the natural trade-offs of system design obsolete.

The objective of this project is to design and characterize multi-stage acoustic filters, delay lines and oscillators. Using the technology available at imec, and especially the sub-micron gap feature of our SiGe-MEMS technology, the candidates will endeavor in the booming field of photonics while enjoying the opportunity of realizing transducers, drivers and sensors, with high electrostatic transduction efficiency. Required simulations will be performed in COMSOL and/or ANSYS (with hands-on training).

Degree:

Master in Science or Master in Engineering, majoring in physics, electronics, mechanics

Type of project: thesis or thesis with internship

Responsible scientist(s):

For further information or for application please contact Xavier Rottenberg (Xavier.Rottenberg@imec.be).

Antenna measurement system for millimeter-waves

The increasing demand on high-throughput wireless communication drives the introduction of wideband millimeter wave solutions such as around 60 GHz. The wavelength reduces to less than one centimeter at frequencies above 30 GHz. At millimeter wave frequencies it becomes therefore possible to integrate antenna arrays in a small-sized wireless system. The radiation pattern measurement of these antennas poses however a serious challenge due to the limited groundplane size in the antennas and due to the high frequency employed.

The objective of this project is therefore the improvement of a new measurement system for the characterization of integrated antennas in millimeter wave systems.

Degree:

Master in Science or Master in Engineering, majoring in physics, electronics

Responsible scientist(s):

For further information or for application please contact Steven Brebels (Steven.Brebels@imec.be).

Millimeter-wave phased-array antennas with polarization agility

The increasing demand on high-throughput wireless communication drives the introduction of wideband millimeter wave solutions such as around 60 GHz. The wavelength reduces to less than one centimeter at frequencies above 30 GHz. At millimeter wave frequencies it becomes therefore possible to integrate phased-array antennas in a small-sized wireless system. Most wireless systems at millimeter wave frequencies use linear polarized antennas. The drawback for handheld devices is its sensitivity to the polarization angle.

The objective of this project is therefore the study and implementation of polarization agility for phased-array antennas in millimeter wave systems.

Degree:

Master in Science or Master in Engineering, majoring in physics, electronics

Type of project: thesis or internship or thesis with internship

Responsible scientist(s):

For further information or for application please contact Steven Brebels (Steven.Brebels@imec.be).

Design of planar metamaterials using transformational electromagnetics

In recent years metamaterials have been developed that offer unprecedented control over electromagnetic fields. In 2006 Leonhardt and Philbin showed that Einstein's general relativity equations provides the theoretical framework for designing devices made of such versatile materials. Given a desired device function, the theory describes the electromagnetic properties that turn the function into reality.

The objective of the study is the design of a planar grid that acts as a metamaterial with an engineerable permittivity and/or permeability tensor. With this grid we want to focus the electromagnetic field coming from one side of the grid towards the other side while preserving amplitude and phase distribution.

Degree:

Master in Science or Master in Engineering, majoring in physics, electronics

Type of project: thesis

Responsible scientist(s):

For further information or for application please contact Steven Brebels (Steven.Brebels@imec.be).

Feasibility of millimeter-waves for thermoacoustic imaging

Thermoacoustic imaging relies on the absorption of electromagnetic energy and the subsequent emission of an acoustic wave (sound). The thermoacoustic process has been first reported by Alexander Graham Bell at the end of the 19th century. Several parts of the electromagnetic spectrum can be used including infrared, microwaves and radio frequencies. Microwave frequencies are suited due to the large contrast in the losses of biologic tissues at microwave frequencies. The imaging resolution at microwaves on the other hand is limited due to the relative large wavelength. Millimeter wave frequencies offer a potential improved imaging resolution.

The objective is therefore to study the feasibility of millimeter waves as an excitation source for thermoacoustic imaging.

Degree:

Master in Science or Master in Engineering, majoring in physics, electronics

Type of project: thesis

Responsible scientist(s):

For further information or for application please contact Steven Brebels (Steven.Brebels@imec.be).

Software and hardware testing platform for an ASIC performing time-of-flight mass-spectrometry

An ASIC that performs mass-spectrometry for space applications has been implemented at imec. The ASIC provides multi-channel front-end amplification as well as time-of-flight measurement. In addition, it can be programmed through an SPI interface.

The student, taking into account current in-house solutions, is asked to develop a reliable Software/Hardware platform to test the ASIC performance. After a preliminary study of the ASIC functionality, the student should define and implement the test platform considering both hardware (PCB design, test equipment) and software (Interface between PC/Data acquisition card and ASIC) requirements.

The student must have a strong background in electronics and in programming (experience with Labview would be welcome). Experience with measurement equipment and PCB design is also required.

Degree:

Master in Engineering, majoring in electrical and electronic engineering

Type of project: internship for a period of at least 6 months. The position is open to Master students at the end of their studies or for PhD students looking for an internship opportunity.

Responsible scientist(s):

For further information or for application please contact Francesco Cannillo (Francesco.Cannillo@imec.be).

Microwave pump/engine

The past years have seen the emergence of new trends in microelectronics. Novel technology drivers and usage scenarios, e.g. low power, nomadism, health care and health monitoring, ..., have led researchers to explore innovative developments paths. Fluidics is one of these.

The spectrum of fluidic applications ranges from adaptive optics, through biological sensing, diagnostics, lab-on-chip, ink-jet heads and tunable RF-devices to nano-particles sorting. At the basis of all these applications resides the controlled displacement of fluids. Therefore, reliable, robust, low power and agile pumps are key components for fluidics applications.

The objective of this work is to study, simulate, design and prototype a pump using microwave transduction as propulsion mechanism. Without any mobile parts, with a low built-complexity and with a good isolation of fluids and excitation, this pump concept promises to depict good reliability at relatively low-cost.

Degree:

Master in Science or Master in Engineering, majoring in physics, electronics

Type of project: thesis or thesis with internship

Responsible scientist(s):

For further information or for application please contact Xavier Rottenberg (Xavier.Rottenberg@imec.be).

Characterization of CNT-based materials

Fullerenes and carbon nanotubes (CNT) in particular, are emerging nano-structured materials with exceptional electrical, mechanical, chemical and optical properties. While their discovery can be traced back at least to the seventies, the continuous improvement of their controlled synthesis allows nowadays considering their widespread implementation on wafer, in coatings and supporting layers. While growth techniques for CNTs have impressively progressed, the precise definition of the CNT properties as well as the uniformity of these needs still studying and optimizing. The statics of the chirality of the CNT's, their single-wall or multi-wall characteristics, their conductivity, ... and the impact of those properties on the macroscopic performance of the CNT-based materials, e.g. in mechanics and microwave domains, are of main interest for their future widespread implementation.

The objective of this project is to assess mechanical and RF-characteristics of CNT-based materials. To this purpose, the student will design effective materials, i.e. CNT patterns embedded or not in polymer matrices, as well as measurement setups (on-wafer, free-space or in-waveguide) to access specific characteristics of these materials. The student will further perform measurements and compare these to simulations of the materials of interest. Particular attention will be given to developing measurement techniques taking the anisotropy of the materials into account.

Degree:

Master in Science or Master in Engineering, majoring in physics, electronics, mechanics

Type of project: thesis or thesis with internship

Responsible scientist(s):

For further information or for application please contact Xavier Rottenberg (Xavier.Rottenberg@imec.be).

III. Smart Systems

Design and analysis of on-chip reliability and characterization circuitry

Each new CMOS technology option and process modification requires thorough characterization of many devices, which is both time and resource intensive. Furthermore, degradation of FET devices during operation also needs to be investigated. This is typically done at accelerated voltages and temperatures.

To facilitate the characterization and reliability tests, circuits designed directly on chip can facilitate and speed up the measurements. For example, a circuit could stress many tested devices in parallel while monitoring their degradation, or poll the tested devices one by one in between stressing to measure the degraded parameters. Challenges include designing circuits that themselves can withstand the accelerated testing conditions and monitor/measure circuits that do not drift.

This project will consist of the initial literature overview, the review of existing test structures and the design phase of new, improved test structures. The student should be proficient in SPICE and CAD layout.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electrical engineering

Responsible scientist(s):

For further information or for application please contact Ben Kaczer (Ben.Kaczer@imec.be) or Geert Van der Plas (Geert.VanderPlas@imec.be).

Integratable organic memory transistors with a polymer ferro-electric gate dielectric

Flash memory devices are widely used in today's electronics. Their working principle is based on a field-effect transistor with a floating gate, on which charges can be stored. By charging or discharging the floating gate, the threshold voltage of the transistor changes and can be read out as a difference in current through the transistor at given bias voltages.

In this master thesis the plastic-technology counterparts of this well-known memory element will be investigated. Organic or plastic semiconductor technology is based on thin-film organic semiconductors. Circuits have successfully been demonstrated, in particular using pentacene as semiconductor. At present there are, however, no examples of circuits comprising re-writeable memory devices. Flash-type transistors are interesting re-writeable memory candidates, in particular when targeting "on-chip" integration with circuits, because their architecture is quite compatible with the transistors used in circuits. However, apart from flash-type memory transistors, several other device architectures and concepts can be imagined to arrive at memory transistors able to store a charge. A possible alternative memory structure is a transistor with a polymer ferro-electric gate dielectric, where the polarization state of the dielectric determines the transistor threshold voltage.

The focus lies on the realization of an integrated organic memory array based on transistors with a ferro-electric gate dielectric and in understanding the charge-storage and polarization-switching concept. By using different device architectures we will try to optimize the device performance. The challenge is to conceive device architectures and concepts that are compatible with circuit technology on foil, both in terms of technology and in terms of programming voltages. The materials we will use to fabricate the devices are polymers as well as organic small molecules. Polymers are typically deposited using spin-coating; small molecules will be evaporated using organic molecular beam deposition. In a first step, single ferro-electric memory transistors will be fabricated and characterized. Subsequently, a process flow will be developed to integrate this organic memory together with existing process flows for organic thin film transistors on foil.

Most of the work will be done in the imec cleanroom. You will receive training on different cleanroom processing equipment (photolithography, wet benches, metal evaporation) and characterization tools.

Degree:

Master in Industrial Sciences or Master in Engineering, majoring in material science, physics, electronics, nanotechnology

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Sarah Schols (Sarah.Schols@imec.be) or Benjamin Kam (Benjamin.Kam@imec.be).

Bottom contacts for improved charge injection in pentacene transistors

Traditional pentacene transistors with gold bottom contacts have been widely investigated during the past and are now used for circuits on plastic foil, aiming an industrial application as for example in plastic RFID tags. Whereas gold has been often used as bottom contact material for historic reasons, it has two practical drawbacks. First at all, the high cost of this noble metal, even used in nanometer thick contacts, can severely inhibit commercial applications. Furthermore, large contact resistance at the gold/pentacene or gold/thiol/pentacene interface can prohibit good charge injection.

Imec is currently collaborating with the Holst Center (The Netherlands) on pentacene transistors aiming high performance and low cost organic circuits for future commercial applications in plastic electronics. In this research imec will investigate various materials for their suitability as bottom contact in pentacene transistors.

The master thesis will focus on characterization of the bottom contacts (for example by optical, and atomic force microscopy), as well as preparation and electrical characterization of pentacene transistors from substrates with various bottom contact materials.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, chemistry, physics, electronics,...

Type of project: thesis or internship or thesis with internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Robert Müller (Robert.Muller@imec.be).

Hyperspectral image processing for cancer detection

Hyperspectral imaging brings great opportunities for many applications, such as early cancer detection and food grading. However, it also brings big challenge for data processing due to the huge amount of data, especially under the constraint of computational power, memory and energy. How to design the image processing algorithms such as image representation, dimensionality reduction and segmentation under these constraints in the context of hyperspectral imaging is not only an interest in the research area, but also a great booster for the applications. The master student is supposed to study this topic following the application-algorithm-architecture co-design principle. Especially, (s)he will investigate its application in cancer detection.

Degree:

Master in Engineering and/or Master in Science majoring in Electrical Engineering or Computer Science. Background in image processing or machine learning is preferred.

Duration: Minimum 5-6 months.

Responsible scientist(s):

For further information or for application please contact Qiong Yang (Qiong.Yang@imec.be).

Ultra-low power programmable processor architecture for 60 GHz digital front-ends

In the domain of multi-gigabits per second wireless 60 GHz communication transceivers and beyond, today's implementations are all based on heavily customized application-specific integrated circuits (ASICs). The basic motivation for this customization is the extremely high processing speeds that are required, in combination with the need for low energy consumption.

However, to support different standards and highly varying usage modes, more programmable or configurable architecture solutions are more attractive. Today these reconfigurable architectures (application specific instruction set processors or ASIPs) are not feasible due to the too high performance/power requirements. Nevertheless, we believe that by introducing and exploiting more dynamic behavior in the digital front-end functionality, the performance/power gap with the ASICs can be largely bridged and potentially even fully overcome. In order to achieve this, innovations are required on the processor architecture side and especially on the way algorithms are mapped to those architectures.

During this internship, the student will first explore input data dynamism as a form of scenario exploitation. Next he will map representative algorithmic blocks onto the chosen ASIP architecture for 60 GHz applications. Then he will generate the VHDL code for the ASIP architecture, followed by synthesis and power estimation of the produced VHDL. These VHDL-level simulations will then allow assessing whether the ASIP can actually beat the ASIC in energy consumption.

After this internship, the student will have acquired a thorough knowledge both on the state of the art in ASIP development and on 60 GHz communications. This experience is highly valuable both in industrial research and development environments as in academic activities.

Profile:

The student should have good knowledge of programming in C and preferably also in Matlab. Knowledge of DSP processor architectures and wireless digital front-end processing are an asset. Strong interest in abstract concepts is essential, in combination with producing simulation-based results to illustrate the concepts.

Degree:

Master in Engineering majoring in micro-electronics or communication systems

Duration: minimum 6 months (full-time, at imec Leuven)

Responsible scientist(s):

For further information or for application please contact Wim Van Thillo (wim.vanthillo@imec.be)

Promoter: Prof. Francky Catthoor (imec-Leuven, K.U.Leuven)

IV. HUMAN++

Heating properties and cell interactions of magnetic nanoparticles

Magnetic nanoparticles have recently attracted a lot of attention because of their potential use in medicine. First of all, magnetic nanoparticles exhibit very interesting magnetic properties not found in the corresponding bulk materials. Secondly, the nanoparticles have controllable sizes ranging from a few up to tens of nanometers. These dimensions are comparable to those of biological entities such as cells, DNA and proteins. The possible interaction between nanoparticles and biological entities opens the door to a variety of promising applications in the biomedical field.

One of the applications drawing specific attention is stem cell based therapies. Within these therapies following the fate and biodistribution of the stem cells in a non-invasive way is of a crucial importance. Magnetic Resonance Imaging (MRI) combined with stem cells labeled with magnetic nanoparticles allows for such in vivo tracking. The magnetic particles induce a hypointense contrast on MR images, thus making it possible to discriminate between the labeled cells and the surrounding tissues. The intensity of contrast produced by the particles is correlated with their magnetic properties. Another possible application of these magnetic particles is hyperthermia based tumor therapy. If the particles are placed in an AC magnetic field, they will produce heat due to Néel and Brown relaxation. This heat can be used in tumor therapy, destroying the tumor cells at higher temperatures.

In this research, a variety of nanoparticles will be investigated for the above mentioned medical applications. Biological modifications of the nanoparticle surface will be explored in order to achieve increased uptake and limited toxicity on the stem cells. Finally, the heating capability of the nanoparticles for hyperthermia upon irradiation with a magnetic set-up will be evaluated.

Degree:

Master in Science, majoring in chemistry, nanotechnology, biomedical science

Type of project: thesis

Responsible scientist(s):

For further information or for application please contact Jesse Trekker (Jesse.Trekker@imec.be), Karolien Jans (janska@imec.be) and Tim Stakenborg (stakenb@imec.be).

Magnetic beads for the combined capturing and detection of biomolecules in blood

Despite great efforts in various application fields, most biosensors have not met the required sensitivity and specificity to allow for label-free detection. The use of magnetic labels may form an interesting alternative to fluorescent or other labels. Not only can the superparamagnetic beads be sensed at very low concentrations, their use for the isolation of cells, proteins or nucleic acids makes it possible to combine sample (pre)purification steps and multiplexed detection on a single portable system with reduced cost. Imec has examined both giant magnetoresistive sensors for detection and current carrying conductors for the manipulation of beads. This thesis will investigate the combination of both techniques for the enrichment and detection of bio-analytes directly from clinical samples. By attracting the beads to the sensor surface to overcome diffusion-limited binding and by integrating all steps into a fully functional platform, higher reproducibility and extremely high detection limits are envisaged.

Students with a chemical background and a high interest in (electronic) engineering are encouraged to apply.

Degree:

Master in Science, majoring in chemistry, bio-engineering or related

Type of project: thesis

Responsible scientist(s):

For further information or for application please contact Frederik Colle (Frederik.Colle@imec.be), Karolien Jans (janska@imec.be) and Tim Stakenborg (stakenb@imec.be).

Measuring molecular binding forces at the nanoscale

The objective of this thesis is to perform a binding force study between biological analytes as a route towards multi-functional, high-throughput biosensing. The study will be performed on an electromagnetic micro chip. An assay will be formed between micro beads and the chip surface by antibody-antigen recognition or between two complementary DNA strands. A repulsive force will then be applied to the micro beads in order to rupture the binding. By monitoring the rupture events either optically or with integrated detectors, the dissociation, hence force, will be recorded in real time. Various types of forces will be tested, e.g. magnetic and dielectrophoretic forces. The heterogeneous combination of different forces may even allow for controllable 3-dimensional bead manipulation. In this thesis, besides performing the necessary binding measurements, the work will also focus on the covalent binding of proteins and DNA to both micro/nano particles as well as sensor surfaces.

Students with a biological or chemical background and a high interest in (electronic) engineering are encouraged to apply.

Degree:

Master in Science, majoring in chemistry, bio-medicine, bio-engineering or related

Type of project: thesis

Responsible scientist(s):

For further information or for application please contact Liu Chengxun (liu.chengxun@imec.be), Karolien Jans (janska@imec.be) and Tim Stakenborg (stakenb@imec.be).

Engineered plasmonic nanostructures for highly sensitive biosensing

Nanostructured metals show some extraordinary properties upon illumination with visible or near-infrared light. So called surface plasmons are the result of a collective excitation of the electrons at the interface between a metal and a dielectric and result in strong resonances in the optical and near-infrared region of the electromagnetic spectrum. These structures are particularly interesting for sensing applications, as the refractive index of the dielectric environment has a strong influence on the resonance position. Small local index variations by molecular binding events can result in measurable shifts of the resonance wavelength. Recently we have demonstrated both special designs that allow facile tuning of the resonance wavelength that are based on a coherent interaction between the plasmonic response of different nanostructures in close proximity, and a new measurement technique enabling a much more sensitive determination of small wavelength shifts.

This project will focus on the application of both the new designs and the novel measurement technique to biosensors. In this project, receptor molecules will first be coupled to the gold metal structures using conventional surface chemistries. After this first immobilization, the binding of the analyte of interest –resulting in a change in dielectric constant– will be monitored in real time. As the influence of binding decreases with increasing distance, different receptor molecules will be tested. The sensitivity of the nanostructures will be assessed and changes to the nanostructure design and measurement setup will be proposed.

Degree:

Master in Science, majoring in nanotechnology, bioengineering, chemistry, biomedical, ...

Type of project: thesis

Responsible scientist(s):

For further information or for application please contact Pol Van Dorpe (Pol.VanDorpe@imec.be) and Tim Stakenborg (stakenb@imec.be).

Perpendicular spin valves

Spin-dependent transport in magnetic multilayers leads to large resistance changes called giant magnetoresistance (GMR) in spin valves or tunnel magnetoresistance (TMR) in magnetic tunnel junctions. These effects are at the heart of applications such as hard disk read heads or non-volatile magnetic random access memories (MRAM), and they are the result of the forces that the magnetic multilayer exerts on the passing current.

The inverse effect also exists, where a spin-polarized current exerts a force on the magnetic multilayer system. This effect is called the spin-torque effect, and it can lead to novel applications such as spin-torque based RF oscillators which are currently being studied at Imec. The magnetization of the magnetic thin films used in these devices usually lies in the plane of the film due to an effect called shape anisotropy. However, films with an out-of-plane magnetization would bring specific advantages such as lower critical current densities and different oscillation modes.

The aim of this project is to develop and optimize the deposition of magnetic multilayers with out-of-plane magnetization. This will be obtained by choosing material combinations with out-of-plane interface anisotropies, while monitoring at the same time that the spin polarization is maintained. The work is mostly experimental and will involve the deposition of the multilayers by sputter deposition, characterization of their magnetic properties by AGFM magnetometry, magneto-optic Kerr effect (MOKE) or magnetotransport measurements, and correlating these with structural properties obtained by X-ray diffraction (XRD) and atomic force microscopy (AFM).

Degree:

Master in Science or Master in Engineering, majoring in electrical engineering, materials science, physics, or related field

Type of project: thesis and/or internship

Responsible scientist(s):

For further information or for application please contact Wim Van Roy (vanroy@imec.be) and Mauricio Manfrini (manfrini@imec.be).

Electrical characterization of cancer cells

Cancer remains a prominent health concern afflicting modern societies. Continuous innovations and introduction of new technologies are essential. As the analysis of circulating tumor cells is most promising in this respect, this thesis aims to develop a device to characterize these cells using electrical impedance spectroscopy. This non-invasive electrical method may provide cell information through permittivity and conductivity measurements of the cell membrane and -cytoplasm. A close interaction of electrodes with the cells lying on top of the device should yield sufficiently high signal to noise ratios and may eventually enable to differentiate various cell subtypes. This is especially promising as most cells that escape from a primary tumor fail to form metastases, and only a minor fraction of circulating cancer cells generally arrest in the microcirculation to form micro metastases of which few persist to form vascularised macro metastases.

Students with a biological or chemical background and a high interest in (electronic) engineering are encouraged to apply.

Degree:

Master in Science, majoring in chemistry, biomedicine, bio-engineering or related

Type of project: thesis

Responsible scientist(s):

For further information or for application please contact Tim Stakenborg (stakenb@imec.be).

Neuronal spike statistical features reliability in dependence of detection and clustering errors

In the course of existing and future work concerning exploration of brain connectivity and information transfer decoding, it is utterly important to have reliable signal processing of neural activity. Information transmitted is somehow encoded in neural activity. Understanding of it is dependant on recording and processing large number of neurons simultaneously. This is done through observation of their extracellular evoked activity potentials – so called spikes. Spikes are thought to be binary activity of neurons which hold the information of relevance in their time intervals of successive appearance. Together, spikes and interspike intervals make spike trains. Detecting spikes and then grouping them by a neuron that “fires” them is called clustering. This is the crucial precondition for spike train analysis.

The goal of this project is to estimate how errors in detection (missed and false detections) and classification (assignment of certain spikes to wrong clusters – treating them as originating from one neuron while they belong to some other) affect parameters extracted from temporal information statistics. This statistics and its parameters (e.g. variability, variance, fast activity (burst) coefficient, pause index, etc.) are used to make certain conclusions about the part of the brain they originate from and are prerequisite to establishment of future closed-loop systems. These systems should create a mechanism to deal with detection of anomalous behavior followed by proper reaction by electrical deep brain stimulation (DBS). Ensuring the safe limits of trust of observed parameters is thus crucial for this purpose.

The student will (with the help of supervisors) work on creating various generated spike trains which will be mixed with realistic noise. Then, some of the existing programs for spike detection and clustering (e.g. Spike2, Osort, Wave_clus) will be used to acquire time-stamps (spike appearance times for each recognized cluster). Then, mentioned features and respective errors will be extracted. This will provide insight of feature reliability which is a crucial element of future systems.

Degree:

Master in Science or Master in Engineering, majoring in electronics, software engineering, signal processing, statistics, ...

Type of project: thesis in cooperation with K.U.Leuven

Responsible scientist(s):

For further information or for application please contact Ivan Gligorijevic (Ivan.Gligorijevic@esat.kuleuven.be) and Wolfgang Eberle (Wolfgang.Eberle@imec.be).

3D registration and visualization of Magnetic Resonance Images

The Bioelectronic system group currently develops an active neurophysiological probe for recording and stimulation of the brain. In the context of the project, such probes are tested in rodents, which are then followed up by Magnetic Resonance Imaging (MRI; see the picture). MRI is an invaluable tool for non-invasive study of the brain. The MRI images have excellent spatial resolution and the potential to differentiate between different tissues (gray matter, white matter, cerebrospinal fluid). In the context of the project, the student will be engaged in development of software tools, in order to facilitate the visualization of the results in 3D.

The student will get familiar with Insight Segmentation and Registration Toolkit (ITK) library (<http://www.itk.org/>) and VTK software package (<http://www.vtk.org/>). The student will implement ITK and VTK bindings for ImageJ, a popular software platform for image processing. The student will demonstrate the use of the plugins using already present experimental data.

Programming skills in high level languages (C++ or Java) are mandatory.

Degree:

Master in Science or Master in Engineering, majoring in computer science, electrical engineering

Type of project: internship (3 to 6 months)

Responsible scientist(s):

For further information or for application please contact Dimiter Prodanov (Dimiter.Prodanov@imec.be).

In vitro biocompatibility of new materials for implantable electrodes

The Bioelectronic systems group develops an active neurophysiological probe for recording and stimulation of the brain in vivo. Current generations of the device have metal contacts, which can be post-processed depending on the specific experiment. Iridium oxide (IrO₂), the carbon nanotubes (CNT) and nanowires (CNW) are promising material for deep brain stimulation electrodes. In the context of the project it is important to assess eventual toxic effects of the materials or the deposition process on the brain neurons. The student will assess the electrochemical properties of the contact material, its transition into the medium, and the eventual toxic effect on the neurons cultured on IrO₂, CNT and CNW films. Depending on the student background and interest, the focus can be more on the biological side or the biochemical/electrochemical side.

Degree:

Master in Science or Master in Engineering, majoring in biomedical sciences, biochemistry, bioengineering

Type of project: thesis (6 months) or internship (3 to 6 months)

Responsible scientist(s):

For further information or for application please contact Danny Jans (Danny.Jans@imec.be) or Wolfgang Eberle (Wolfgang.Eberle@imec.be).

The bio-electronic nose: immobilisation of olfactory neurons on microchips

The electronic nose is a device for analyzing volatiles. The goal of this system is to imitate the human odor reception. The nose comprises sophisticated hardware with sensors, electronics, pumps, air conditioning systems and control systems (analogous to the biological nose with the olfactory epithelium). On the other side, it also comprises software for hardware control and data analysis. These devices are being used in the food industry, medical industry and environmental technology.

Although there has been a great improvement in the electronic nose technology, the sensors can hardly reach the performance of their biological equivalent, the human nose. This defines the basis of the research on the development of a bio-electronic nose, in which olfactory mouse neurons are being used as sensors. These are put in culture on micro-electrodes with which their electric activity can be recorded. In the context of this research, a master thesis topic is defined for the student. The practical work comprises in a first phase the setup, follow-up and evaluation of the olfactory neuron culture with cell stainings specific for the neurons and receptors. In a second phase, the cellular reactions on odorants and other reagents are being investigated by fluorescence microscopy and measurements on chips with micro electrode arrays (MEAs).

Degree:

Master in Bio-Engineering, majoring in bio-engineering, biomedicine

Type of project: thesis in cooperation with K.U.Leuven, dep. MeBioS

Responsible scientist(s):

For further information or for application please contact Evelien Micholt (Evelien.Micholt@imec.be) and Wolfgang Eberle (Wolfgang.Eberle@imec.be).

Wireless sensor nodes for Electrocardiogram (ECG) signal monitoring and analysis

The ever increasing interest towards smarter, smaller, and autonomous wearable health monitoring for medical and lifestyle applications is driving the research for the realization of ultra-low-power and wireless sensor nodes. These sensor nodes will be responsible for extracting medical signals from the patient and process them to detect the presence medical disorders.

Imec has been developing such sensors nodes more than 10 years combining our world leading research on each and every building block of wireless autonomous sensor nodes.

An important part of our research focuses on the development of algorithms. Standard algorithms are consuming considerable power when integrated into our low-power sensor nodes. Imec has already been developing the first version of such low-power algorithms.

The responsibility of the student in this thesis will be (a) Evaluate the reliability of our present algorithms in real-life tests using our sensor nodes, (b) Define possibilities for improving the reliability of these algorithms, (c) Integrate the improved algorithm into our sensor nodes (embedded C programming is required), (d) Evaluate the reliability of the new system in real-life tests.

Following skills are required for the applicants (a) Result driven research skills, (b) Experience in Matlab and C++ programming, (c) Very good knowledge in signal processing, (d) Very good understanding of electronics systems hardware (i.e. electronics system design).

Degree:

Master in Engineering, majoring in electrical and electronics engineering, biomedical engineering

Type of project: thesis or internship with a minimum study duration of 6 months

Responsible scientist(s):

For further information or for application please contact Refet Firat Yazicioglu (firat@imec.be) and Tom Torfs (torfst@imec.be).

V. Energy

Extreme UV imagers

Solar blind UV detector devices are considered by the European Space Agency (ESA) as appropriate devices for applications in the extreme ultra-violet on their next solar mission (solar orbiter). Compound semiconductors of the III-nitride material system (e.g. $\text{Al}_x\text{Ga}_{1-x}\text{N}$), spanning band gaps from 3.4 to 6.2 eV, are promising candidates for solar blind UV detector devices. The aim of this investigation is to fabricate a 2-D pixel array camera, for the extreme ultra-violet band using those materials. To realize this challenging aim, novel detector interconnect concepts have been studied and devices have been fabricated. The objective for the student in this thesis subject is to continue the currently on-going research by contributing on the fabrication of those detectors and by studying their process optimization. That includes experimental work (using imec's clean room facilities) as well as electro-optical characterization (I-Vs, photoresponse measurements) and analysis of the results. Characterization at ESA laboratories is also a possibility, after detector's successful fabrication and testing in-house.

Degree:

Master in Science or Master in Engineering, majoring in electrical engineering, physics

Type of project: thesis and/or internship

Responsible scientist(s):

For further information or for application please contact Kiki Minoglou (Kiki.Minoglou@imec.be).

Proof-of-concept and optimization of tunneling barriers in standard silicon solar cells

Photovoltaic is a fast growing field, dominated by crystalline silicon solar cells. Yet there remains a significant difference between the theoretical efficiency one could reach and the efficiency actually reached with these cells, and this both in production lines and in laboratories. Part of the efficiency loss comes from the interface between silicon and the metallic contacts of the cell: at this interface, light-generated free carriers recombine without being collected by the cell contacts. To reduce the recombination rate, it has been suggested to include a thin dielectric layer, a so called tunneling barrier, between silicon and the metallic contact. If well chosen, this dielectric leads to a reduction of the recombination rate. At the same time, the dielectric layer should be thin enough to allow for tunneling of the charge carriers through it. While it has already been shown that tunneling barriers can lead to an efficiency increase, the objective is here to include these barriers in industrial-type solar cells.

Your objective in this work will be the development of tunneling barriers. First, a proof-of-concept should be obtained on small size standard solar cells. Then, the process will be adapted in order to be applied on larger cells, and with different metallization techniques.

This work will mainly be experimental. You will join a team of scientists from all around the world to work in laboratories and cleanroom for processing solar cells and various structures, characterizing them and analyzing your results. Besides this practical work, you will perform simulations of solar cells with a dedicated software in order to improve our understanding of tunneling barriers. You should have a liking for lab-work and a good knowledge of written and spoken English.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in physics, materials science, nanotechnology, ...

Type of project: thesis or internship or thesis with internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Xavier Loozen (Xavier.Loozen@imec.be) and Ivan Gordon (Ivan.Gordon@imec.be).

Development of heterojunction solar cells with rear emitter and rear contacts

Heterojunction emitters which consist of amorphous silicon deposited on a crystalline silicon substrate, provide a route to obtain high efficiency solar cells, as demonstrated by the 23% efficiency cells reported by Sanyo. Promising as these results are, these structures are fundamentally limited by the metal placed on the front of the solar cell, and the light absorption in conductive oxides which are also used. Placing both metal contacts on the rear of the structure enables higher short circuit current values to be obtained, and when coupled with the high open circuit voltage possible with a heterojunction emitter, provides the potential for realising high efficiency solar cells.

The aim of this project is to contribute to the ongoing efforts in imec on development of technologies to enable such structures, and in particular to passivation layers between the crystalline silicon and the metal contacts. It is envisaged this will involve process development for intrinsic and highly doped amorphous silicon layers, to be selectively inserted between the crystalline substrate and the metal electrode. This work will involve optimising etching processes to be used in patterned silicon wafers, and the choice of metal(s) to be deposited to realise the contacts. The research will involve design of experiments, leading to full solar cell fabrication - from bare silicon wafers, to the final measurement of electrical characteristics of the device.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electronics, material science, ...

Type of project: thesis or internship for a period of minimum 6 months

Responsible scientist(s):

For further information or for application please contact Barry O'Sullivan (Barry.OSullivan@imec.be) and Ivan Gordon (Ivan.Gordon@imec.be).

Simulation of the influence of grain size distribution and stress in polycrystalline silicon layers on the solar cell performance

To increase our knowledge of thin film solar cells we are looking for a motivated student. She or he will simulate the influence of grain size distribution and stress present in thin polycrystalline silicon layer on the final solar cell characteristics.

The relatively new “thin-film polycrystalline-silicon (grain size of 0.1-100 μm) solar cell on foreign substrate” technology aims at low-cost devices with energy conversion efficiencies above 12%. At imec different methods to fabricate such polycrystalline layers are investigated. In the past we build up knowledge by correlating the experimentally measured material and solar cell characteristics. However due to experimental limitations and the influence of many external parameters such correlation is not always straight forward. Therefore device simulations of our solar cells are an attractive and complementary approach to improve our knowledge, which in the end will lead to higher efficient solar cells.

Amongst others the grain size distribution and stress present in the polycrystalline silicon layers is depending on the fabrication method and process parameters used. Via simulations using a powerful circuit simulator such as SPICE, you will investigate the influence of one of the two or both parameters (grain size distribution, stress) on the solar cell characteristics. The purpose is to develop a distributed SPICE-model for a solar cell. This multi diode model can tell use more about the influence of the smallest grain on e.g. the open circuit voltage. Experimentally we found a correlation between the stress present in the polycrystalline silicon layers and the open circuit voltage. By simulations we try to figure out to which extent this effect can be explained via bandgap narrow.

You will use the experimental data of your colleague researchers in your own models. Therefore we are looking for a motivated student with good computer knowledge and a strong interest in device physics simulations.

Degree:

Master in Science or Master in Engineering, majoring in material science

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Ivan Gordon (Ivan.Gordon@imec.be) and Yu Qui (Yu.Qiu@imec.be).

Optimization of TCO coating for heterojunction and thin-film Si solar cells

TCO coating is important for thin-film Si solar cells and for wafer-based a-Si/c-Si heterojunction cells. Both types of solar cells are studied in-depth in the solar cell group at imec. In order to improve the efficiency of these types of solar cells, a highly transparent and conducting coating is needed for anti-reflecting and contacting purposes. Typical TCO's used for solar cells are aluminum zinc oxide (AZO) and indium tin oxide (ITO). Besides the optical and electrical properties of the TCO layer itself, the chemical/thermal compatibility and the possible impact of the TCO deposition on the solar cell performance are of interest. We have recently acquired a high-throughput sputtering system for deposition of TCO's on thin-film Si solar cells and heterojunction solar cells.

During the assignment you will (help to) develop and optimize the TCO sputtering processes. In order to do this, you will carry out sputter process optimization, uniformity and morphology studies, optical and electrical characterization, post-annealing experiments, and comparison of different target materials. The preliminary task is to improve the conductivity, transmission and homogeneity of the TCO layers while keeping the deposition process compatible with our low-temperature cell processing. Solar cells will be made to assess the influence of TCO layers at cell level. You will also evaluate possible contamination problems and determine the impact of this on the efficiency of solar cells. Based on your work, a proposal for optimized sputter and post-anneal processes will be made.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, physics, chemistry, electronics, ...

Type of project: internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Ivan Gordon (Ivan.Gordon@imec.be) and Yu Qui (Yu.Qiu@imec.be).

Wet chemical texturing and cleaning for solar cell processing

In order to improve the efficiency of solar cells, the surface of the cells is usually modified to absorb as much light as possible. One technique of doing this is by roughening the surface in a wet chemical bath. This roughening is done at the beginning of the fabrication process. After the roughening process, the surface needs to be cleaned and passivated before the solar cell structures can be made. We have found indications that the efficiency of the cleaning step is very important in determining the properties of the solar cell.

During the assignment you will (help to) develop the cleaning step after roughening in different alkaline chemistries. In order to do this, you will carry out roughening and cleaning experiments in our labs. You will evaluate residual contamination after cleaning and determine the impact on the efficiency of solar cells. Based on your work, an evaluation will be made of the different etch and clean chemistries that are available.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in chemistry, material science, ...

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Twan Bearda (Twan.Bearda@imec.be).

Wet chemical passivation of silicon surfaces for solar cell processing

One of the most important parameters of a high efficiency solar cell is the lifetime of charge carriers (electrons, holes) that are generated by light. In the presence of defects at the surface, many of these charge carriers recombine. This results in a low lifetime and therefore in a low solar cell efficiency. For this reason, passivation ('repair') of these defects is very important. One way of doing this is by wet chemical treatment. In the assignment you will carry out experiments to evaluate different approaches to wet chemical passivation. The purpose is to improve the quality of passivation as well as its stability. You will determine the quality of passivation directly by measuring the charge carrier lifetime, and indirectly by determining functional groups at the surface using infrared absorption. You will also evaluate the importance of wet chemical treatment in combination with subsequent process steps. Based on your work, a proposal for an optimized fabrication process will be made.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in chemistry, physics, material science, ...

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Twan Bearda (Twan.Bearda@imec.be).

Thin-film polycrystalline-silicon layers made by solid phase crystallization or aluminium-induced crystallization for solar cells

The relatively new "thin-film polycrystalline-silicon (grain size of 0.1-100 μm) solar cell on foreign substrate" technology aims at low-cost devices with energy conversion efficiencies above 12 %. Direct deposition of silicon on a non-silicon substrate results in amorphous or small-grained material. To fulfill the demand of relatively large grains, different methods to (re)crystallize Si are investigated at imec namely aluminum-induced crystallization (AIC) and solid phase crystallization (SPC). The absorber layers of our solar cells are formed by a two step process of seed layer formation, via AIC or SPC, and epitaxial growth on top. Recently we showed that the efficiency of such solar cells is limited by electrically active intragrain defects present in the absorber layer. The electrical activity of these defects can be triggered by (metal) impurities. Depending on your interest and the current state of the art, both or one of the two following topics will therefore be studied. 1) Defects: The origin of the defects present in the absorber layers lies in the seed layer. You will study and try to reduce the defect density in both types of polycrystalline seed layers by investigating the influence of different parameters on the crystallization process. 2) Contamination: Due to the different approach and systems used for both crystallization technologies the (metal) impurity concentration is different. You will study the influence of impurities on the solar cell performance by comparing both types of solar cells and try to reduce the impurity concentration. The project has a clear experimental character. You will be involved in many steps of the polycrystalline solar cell fabrication process as well as in the characterization. Therefore we are looking for a motivated student with a hands-on mentality, capable to do independent research.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electronics, physics, material science, ...

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Dries Van Gestel (Dries.Vangestel@imec.be) and Ivan Gordon (Ivan.Gordon@imec.be).

Investigations on advanced emitters in next generation silicon solar cells

Crystalline silicon solar cells have a market share of more than 92% in roof top installations. While the standard thickness in production nowadays is at $\sim 180 \mu\text{m}$ ($156 \times 156 \text{ mm}^2$), the solar cell roadmap is directing towards thinner and thinner cells by further increasing the efficiency in order to reduce the cost/Wp. Within the imec Photovoltaic department new fabrication processes are developed to provide thinner cells, requested for future production.

Novel emitter structures with consequently novel metal contact schemes have to be developed. For that different kinds of emitter profiles are investigated and front side metallization concepts are studied. The student will be part of the Industrial Solar Cell Team and actively participate in these novel developments.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electronics, physics, material science

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Joachim John (Joachim.John@imec.be).

Investigations on advanced rear-side passivation in next generation silicon solar cells

Crystalline silicon solar cells have a market share of more than 92% in roof top installations. While the standard thickness in production nowadays is at $\sim 180 \mu\text{m}$ ($156 \times 156 \text{ mm}^2$), the solar cell roadmap is directing towards thinner and thinner cells by further increasing the efficiency in order to further reduce the cost/Wp. Within the imec PhotoVoltaic department new fabrication processes are developed to provide thinner cells, requested for future production.

In the framework of reducing the thickness of the silicon substrates the influence of the rear-side surface recombination becomes important. Already at silicon solar cell thicknesses of $150 \mu\text{m}$ the rear-side surface recombination current participates in the loss current and leads to degradation of the cell performance. Novel back-side passivation materials like e.g. AlO_x are investigated on surface passivation. Novel passivation materials are benchmarked against existing passivation schemes like thermal SiO_x .

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electronics, physics, material science

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Joachim John (Joachim.John@imec.be).

Investigating various front and rear contact screen printing pastes for n-type multi-crystalline Si rear junction cells

Shallow front surface field is needed to enhance the blue response of the n-type mc back junction cells. This requires investigation of various Ag front contact pastes, which can contact lowly doped front surface field. The conventional screen printing pastes are designed for shallow diffusion in front junction p-type cells to avoid shunting of the p-n junction. N-type cells have the advantage of p-n junction being at the rear of the cells, thus even a deeper diffusion of the paste may not cause any shunt. It could be possible to contact much shallow and lowly doped n^+ region by deeper diffusion as compared to p-type cells.

The p-type emitter in these cells is created by firing of screen printed Al, resulting in Al alloying. However, the peak concentration of Al in these cells is limited by its solubility limit. Adding boron to the screen printing paste could lead to higher doping of the emitter. Thus Al-B pastes with different content of boron will be compared with standard Al pastes.

Recently, new Ag and Al screen pastes have been received from Ferro and DuPont. These following pastes will be studied as a part of above project. In addition to the electrical characteristics, cells will be studied by SEM and ECV studies.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electronics, physics, material science

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Sukhvinder Singh (Sukhvinder.Singh@imec.be).

Characterization of solar cells for indoor applications

The number of electronic devices per person has been steadily increasing over the last few years. This trend is bound to continue, with the emergence of very small electronic appliances distributed over our living environment and on the human body, providing functions enhancing comfort, safety and health (example : small glucose level monitoring system for diabetes patient). All these ambient intelligence applications however need power, to function and to communicate (powering a display or sending a radio signal). The distributed nature of these small systems makes traditional power supply through hard wires in the best case impractical and in most cases impossible. Primary (disposable) batteries are not applicable because of the limited autonomy and are not desirable from the environmental point of view. A number of ambient energy technologies already exist or are under development. However most of them suffer from a low energy density (less than 200 J/cm³/year). Solar cells are an appealing exception, with indoor energy densities easily one order of magnitude over this figure. The standard solar cell I-V measurement setup has been established for a long time. However, there is no specific solar cell characterization tool for the indoor application. The purpose of this internship topic is to search for the proper method which can offer efficient information on the cell performance under different injection level, especially for the indoor application. The aim is to build a characterization setup able to measure solar cells under typical illumination conditions as found in office buildings. The realized setup will be assessed by performing IV measurements, measuring cells under varying conditions (types of lamps and distance of the lamp to the cell) and comparing the cell results with data from other groups.

Timeline:

Month 1-2: Learn about solar cells and their application in indoor applications - Get acquainted with the issues in characterization of solar cells for indoor applications - Perform IV measurements with the standard IV characterization setup - Start construction of new characterization setup

Month 3-4: Finalize characterization setup - Start characterization of indoor solar cells - Perform characterization experiments with varying types of lamps and varying distances

Month 5-6: Finalize characterization experiments with varying types of lamps and varying distances - Make procedure for standardized indoor PV characterization - Write final thesis report

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electronics, physics, material science

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Chun Gong (Chun.Gong@imec.be) and Niels Posthuma (Niels.Posthuma@imec.be).

Development of parallel gap welding interconnect solutions for innovative photovoltaic modules

Photovoltaics is considered as an important solution towards the future generation of renewable, generation energy. Within this field, imec plays an important role in the development of innovative solutions for the further enhancement of solar cells. Amongst the subjects under study are the development of solar cells with a strongly reduced thickness, both using the classical Si semiconductor material as well as III-V semiconductor materials applied in high-efficiency concentrator PV applications. In both cases, the integration of individual cells into solar modules will require the development of innovative technologies for contacting and interconnection of these cells. Parallel gap welding, a well established technique for integration of solar cells into modules for space applications, offers an interesting solution, but requires an optimization for the specific layout and parameters of the solar cells currently under study.

This project will offer the involved student a good insight into the production process of innovative photovoltaic cell solutions, and hands-on experience with an important step towards module integration of these cells and characterization of the resulting assemblies.

During 2010 an investment is planned in a new parallel gap welding tool, to be used for HFD and U-module work. A screening and optimization of the different possible module integration solutions offered by this tool will be required.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, physics

Type of project: thesis starting in July/August 2010

Responsible scientist(s):

For further information or for application please contact Giovanni Flamand (Giovanni.Flamand@imec.be).

Development of characterization tools for innovative high-efficiency concentrator photovoltaic cells

Concentrator PhotoVoltaics (CPV) is an emerging and promising alternative photovoltaic solution for the generation of renewable electricity. The use of high-efficiency multijunction solar cells in combination with concentrating optical elements offers high nominal power output and competitive €/W figures.

Standard characterization of solar cells and modules is performed by measuring the IV-curve of the device while illuminated by a solar simulator source, mimicking the standard solar irradiation. Standard systems, like the ones available in imec, are equipped for the characterization of relatively big solar cell devices under normal irradiation. Solar cells for CPV applications however typically are very small (mm^2 -size) and ideally are characterized under highly concentrated illumination (500-1000 suns). The subject of the present topic is the development of a suitable solution for contacting small area solar cells allowing a fast and accurate characterization, both under standard 1-sun and highly concentrated sunlight conditions. This study will offer the opportunity to gain insight into the development process of an innovative solution in the field of photovoltaics, and specifically a detailed knowledge on important aspects of solar cell and module characterization. An ideal candidate for this position combines a good theoretical and practical knowledge of basic electrical and optical systems with a hands-on solution oriented approach.

Mechanically stacked multijunction devices are to become available in high quantities during the next couple of months, but a workable solution for their characterization is not available in-house at the moment.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electronics, material science

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Giovanni Flamand (Giovanni.Flamand@imec.be).

Integration of solar cells into flexible modules

In the SCT (Solar Cell Technology) group of imec, advanced silicon solar cell concepts are investigated and developed, in view of the growing demand for sustainable energy. Of course, cost is an important driver and one of the routes pursued by the group to lower production costs for solar panels is by decreasing the cell thickness, since the amount of silicon is still an important part of the total module cost. Going to ever thinner cells, however, also impacts processing technology, as thin silicon is very brittle and fragile, and highly susceptible to breakage during handling.

In this view, there is a growing demand for packaging technologies that can protect those cells during, but definitely also after processing. Additionally, such a packaging technology should allow interconnection of several cells into a single so-called module. Lately, the SCT group has started up activities on such modules to meet this demand, and a first technology has already been demonstrated as proof-of-concept. This so-called U120 technology embeds and interconnects back-contact solar cells in silicone on a glass substrate (through which they are illuminated). The goal of this thesis is to implement this technology on flexible substrates, investigate the possible advantages of such a switch, e.g. flexibility (possibly resulting in an improved reliability concerning impact), light-weight (lowering the load on roof-mounted panels), thinness (space savings), rollability/foldability (for transport or mobile applications), processing throughput, and weigh them up against the drawbacks that may turn up, e.g. increased fragility of embedded cells (cracking), adhesion issues (delamination of the substrate), a decrease in optical performance (due to worse transmission of the substrate), higher susceptibility to moisture uptake... Depending on the thickness of the embedded cells and encapsulation layers (adhesives and substrates), and the strength of the interconnections (adhesion and yield strength), the resulting module can be fully flexible or foldable.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, physics, electronics

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Ivan Gordon (Ivan.Gordon@imec.be) and Jonathan Govaerts (Jonathan.Govaerts@imec.be).

Low-temperature metallization for heterojunction solar cells

Heterojunction emitters which consist of amorphous silicon deposited on a crystalline silicon substrate, provide a route to obtain high efficiency solar cells, as demonstrated by the 23% efficiency cells reported by Sanyo. However, the presence of amorphous silicon introduces some complexities to processing, in particular to the maximum temperatures to which the samples can be exposed. The amorphous silicon can (partially) crystallise when subjected to high temperatures, and its electrical characteristics are severely degraded in such cases. This means the metallisation to create the two electrical contacts cannot be performed by the standard screen printing and high temperature firing process.

The aim of this work is to develop processes for creating the metal contact to the base and emitter regions of heterojunction solar cells. The processes to be used are screen printing and aerosol jetting. Such processes are possible as the pastes that are used are compatible with the temperature requirements of such devices, and can ensure a highly conductive contact to silicon at low temperature. This work will involve developing processes for the deposition, annealing and characterisation of the metal lines. This will be done both on solar cell level, and on specially designed test structures.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in electronics, material science, chemistry, ...

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Ivan Gordon(Ivan.Gordon@imec.be) and Barry O'Sullivan (Barry.OSullivan@imec.be).

Optimization of a nanoimprint process for thin-film silicon solar cells

The abundance of solar energy gives to photovoltaic devices the brightest future of all renewable energies. But unfortunately, if solar energy is free, solar cells are not. Their biggest challenge is to reach more competitive prices. For that reason, the fabrication of solar cells has to rely on processes that provide high throughputs at low cost. This means that high-performance but expensive processes like optical lithography for meso- and nanostructures cannot be used. To achieve such structures, nanoimprint lithography (NIL) is a promising low-cost alternative, by which the pattern transfer is realized by pressing a patterned mold onto a resist-coated wafer. The imprinted resist can then play the role of a mask for etching the wafer. Such a process is currently being developed at imec for the fabrication of ultra-thin films for solar cells and it is also of interest for fabricating light-trapping schemes, to improve the performance of these ultra-thin cells.

Your objective in this work will be to improve and broaden our current NIL process by optimizing the parameters and by exploring new resist materials and routes. Not only will you work on NIL but also on etching techniques (e.g. reactive ion etching, anodisation) in order to realize the complete pattern transfer and eventually test the structures on devices.

Apart from a broad literature review, this work will mainly be experimental. You will join a team of scientists from all around the world to work in laboratories and cleanroom for processing polymers and semiconductors, characterizing the fabricated structure and analyzing your results. You should therefore have a liking for lab-work and a good knowledge of written and spoken English.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in materials science, chemistry, nanotechnology, ...

Type of project: thesis or internship or thesis with internship for minimum 9 months

Responsible scientist(s):

For further information or for application please contact Ivan Gordon (Ivan.Gordon@imec.be) and Valerie Depauw (Valerie.Depauw@imec.be).

Characterization of epitaxial layers as emitters and BSFs for silicon solar cells and optimization of the epitaxial deposition process.

Silicon solar cells are semiconductor devices that operate by converting sunlight directly into electricity. Broadly speaking, the most common type of silicon solar cell consist of a p-n junction that allows current to flow in one direction while blocking current flow in the other direction. A scheme of the basic structure of a silicon solar cell is shown in **figure 1**.

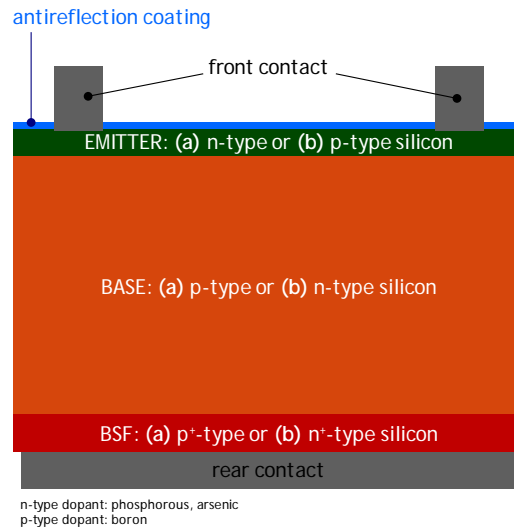


Figure 1. Cross section of the basic structure of a silicon solar cell with a front side emitter: **(a)** n-type emitter and p-type base, **(b)** p-type emitter and n-type base.

The emitter and the base of a silicon solar cell make up the p-n junction, and the back surface field (BSF) consists of a heavily doped region located right at the back contact of the solar cell which contributes to reduce recombination velocities in the region.

Currently, the industrial emitter formation in a solar cell is mainly made by diffusion of phosphorous with POCl_3 as precursor. Nevertheless, a promising mid-term alternative for the emitter formation is the epitaxial growth by chemical vapor deposition (CVD) of chlorosilanes. CVD allows a very controllable formation of the emitter with the desired thickness, doping and profile. This is a big advantage, compared to the more limited flexibility in the design of a diffused emitter, which opens new opportunities in the solar cell design. Moreover, the work performed until now on silicon solar cells with epitaxial emitters shows outstanding results regarding their performance in the short wavelengths (blue response). As a result, there is a growing interest in the incorporation of epitaxial emitters in silicon solar cells, technology that can also be applied in the formation of the BSF. Nowadays, the screen printed aluminium BSF is the option most widely applied to industrial silicon solar cells. The screen printed aluminium-BSF is realized on structures which already have an n⁺-p junction at the rear of the solar cell due to the diffusion of the phosphorus in both sides of the wafer during the emitter formation. The actual formation of that BSF takes place in the firing step applied to create the front and the back metal contacts during the metallization by screen-printing.

At the moment, the main challenge regarding the implementation of epitaxial emitters and BSFs into the solar cell industry is the lack of a high throughput and low cost CVD system. The commercial systems presently available are single wafer tools, which are not an option for the photovoltaic industry.

In the scope of this field imec, in collaboration with tool manufacturers, has initiated a joint research project. In particular, we are working in the hardware and process development of a potentially high-throughput CVD system for the formation of epitaxial emitters and BSFs for silicon solar cells. The tool is already installed at imec, and the

goal of the project is not only to improve the hardware but also to develop a suitable process for solar cells application aiming at throughput, low cost and good quality layers.

The work to be done during the master thesis/internship will take place within the process start-up and development of the CVD system mentioned above. The main tasks covered by this work are the following:

- 1) Characterization of the deposited layers by techniques such as SIMS (secondary ion mass spectrometry: compositional depth profiles), SRP (spreading resistance probe: resistivity and carrier depth profiles), 4 point probe (sheet resistance), TXRF (total reflection X-ray fluorescence: surface metal contamination), SPV (surface photovoltage: bulk (Fe) contamination), SEM (scanning electron microscope: thickness and further inspection of the layer quality), optical microscope inspection (inspection of the layer surface), defect etching (quantification of the layer quality), FTIR (Fourier transform infrared reflectance: layer thickness) and ellipsometry spectrometry (layer thickness).
During this project, depending on the time availability and feasibility, the student will learn to perform by himself/herself some of the previous characterization techniques.
- 2) Interpretation of the results obtained from the analysis mentioned above.
- 3) Taking into account the results obtained in the characterization step, improvement of the deposition conditions (flows, times, pressure, temperature, times...) to get layers with the suitable quality and profile for solar cell application.
- 4) Processing of solar cells including epitaxial emitters or BSFs in an industrial solar cell flow.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in material science, physics, electronics engineering, chemical engineering...

Type of project: thesis or internship or thesis with internship for minimum 9 months

Responsible scientist(s):

For further information or for application please contact Maria Recaman Payo (recaman@imec.be) or Frederic Dross (dross@imec.be).

Metal seed layer for shallow non-selective emitters

The aim of this activity is to study selected silicide as a seed layer to be used to contact a non-selective shallow (200-300 nm) emitter for crystalline WEpi (wafer equivalent epitaxial silicon solar cells). This is oriented to alternative metallization schemes in which no silver is used but e.g. Cu. The final metallization process should be a good choice a front contact for an industrial solar cell. A silicide is preferred as a seed layer because of mechanical properties (adhesion) and for electrical reasons (contact-resistance). If an alternative non-silicide material exists with good adhesion, a good contact resistance and resulting in a self-aligning process, this can also be considered. The seed layer should be suitable to be a starting layer for Cu electroplating. This implies the adhesion of the seed layer is sufficiently good to avoid lift-off after plating a 10 to 20 μm thick Cu layer. Furthermore the silicide should be a barrier against copper diffusion.

The student will be involved in the characterization of the selected silicide compositions to be applied in WEpi (wafer equivalent epitaxial silicon cells) but also in searching for alternative non-silicide materials for the same purposes of seed layers. The characterization will include contact resistance measurements and penetration depth. Based on the results of the characterisation, a method for a self aligning seed layer process will be developed for the selected silicide. This will be either based on electro-less plating and/or on selective etching of non-silicided metal. In this sub-task the student will have opportunity to study in depth electro-less metal depositions and electro-less Cu plating. Obtained layers will be characterised in terms of uniformity, sheet resistance, and reliability.

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in chemistry, physics, material science

Type of project: thesis and/or internship

Responsible scientist(s):

For further information or for application please contact Frederic Dross (dross@imec.be) and Isabela Kuzma (kuzma@imec.be)

Module design of organic photovoltaic cells

The efficiency of organic solar cells increases yearly, with top values of single cells close to 8% achieved recently. These numbers make it possible to go for commercial products, competing with more traditional photovoltaic materials. An important step towards commercialization is connecting different single cells in a module. During the project, you will go through all the different steps of module fabrication: simulation, deposition, patterning and measurement. Simulations give an insight in the optimal module configuration, depending on certain parameters. These parameters (produced power, resistance of the contacts, shadow losses) are measured, and iterated to the simulation software. The fabrication of the module involves the usage of different layers, consisting of metals and organics, on top of each other. As several cells need to be connected to each other, patterning of the layers is a key issue. Your task is finding the best processing conditions and patterning techniques to minimize the losses induced by the interconnection of the single cells.

Work load: Literature study 20% - Simulations 20% - Experimental work: 60%

Degree:

Master in Industrial Sciences or Master in Science or Master in Engineering, majoring in physics, electronics

Type of project: thesis or internship or thesis with internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact David Cheyns (David.Cheyns@imec.be).

Towards increased air stability of organic solar cells

Plastics are known to be insulator but this is about to change with the emergence of organic electronics. Some applications of organic electronic have been already commercialized, for example organic light emitting diodes and many others will appear in the coming years. Polymer solar cells are one of the most promising applications of these new versatile organic semiconductors. These solar cells could be lightweight, inexpensive and very practical. However several challenges must be overcome before these photovoltaic devices can be considered as a truly practical technology. Over the last years impressive progress has been achieved in organic photovoltaic device efficiency and promising roll-to-roll compatible deposition techniques have been also reported. This rapid technological development brings applications close-by, and consequently also the importance of device reliability. Concomitantly R&D should focus on the understanding and description of fundamental degradation mechanisms and development of low-cost and effective encapsulation technologies. The packaging should respect stringent requirements in terms of permeability to humidity, oxygen and UV light and at the same time adapt to the device architecture. Other requirements arise to maintain the competitive arguments of organic solar cells compared to inorganic technologies, namely, flexibility, low-cost and production upscaling ease.

One of the biggest challenges of encapsulation technology development lies in the measurement of low water transmission rates required by organic electronics devices as the commercially available Mocon test's sensitivity is insufficient. Therefore the focus of this master thesis lies in the implementation of a Calcium test, which is based on the oxidation of the thin evaporated calcium layer in presence of oxygen and humidity. During the oxidation the reflective calcium evolves to an increasingly transparent layer of calcium oxide. Currently, Calcium test is only done by a visual inspection and only gives qualitative results. However this technique bears the promise of a highly sensitivity and quantitative characterization technique, if appropriate image analysis is developed. The student after training on the calcium sample preparation and encapsulation will focus on the implementation and calibration of the measurement setup, therefore interest in scientific instrumentation and image analysis is an advantage.

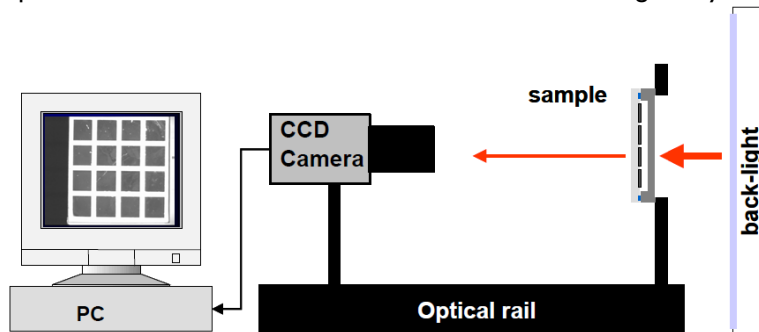


Figure 1: Standard Calcium test setup

Degree:

Master in Industrial Sciences and/or Master in Engineering majoring in electronics, instrumentation, physics, material science.

Type of project: thesis or internship for minimum 6 months

Responsible scientist(s):

For further information or for application please contact Soeren Steudel (soeren.steudel@imec.be) and Eszter Voroshazi (eszter.voroshazi@imec.be).